

N and P Channel Enhancement Mode Power MOSFET

Description

The 6706A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

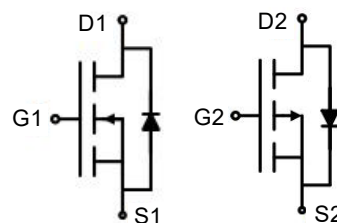
General Features

- NMOS
- V_{DS} 30V
- I_D (at $V_{GS} = 10V$) 6.5A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 20m Ω
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 30m Ω
- 100% Avalanche Tested
- RoHS Compliant

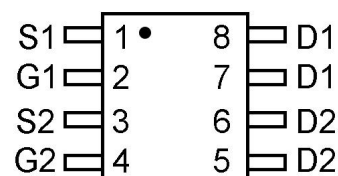
- PMOS
- V_{DS} -30V
- I_D (at $V_{GS} = -10V$) -5A
- $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 45m Ω
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 70m Ω
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



pin assignment



SOP-8 Dual

Ordering Information

Device	Package	Marking	Packaging
6706A	SOP-8 Dual	6706	4000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Continuous Drain Current	I_D	6.5	-5	A
Pulsed Drain Current (note1)	I_{DM}	26	-20	A
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Power Dissipation	P_D	2	2	W
Single pulse avalanche energy (note2)	E_{AS}	9	14	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	62.5	62.5	$^\circ\text{C/W}$

NMOS Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	1.5	2.0	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 5A	--	16	20	mΩ
		V _{GS} = 4.5V, I _D = 5A	--	24	30	
Forward Transconductance	g _{FS}	V _{GS} = 5V, I _D = 5A	--	15	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz	--	479	--	pF
Output Capacitance	C _{oss}		--	68	--	
Reverse Transfer Capacitance	C _{rss}		--	59	--	
Total Gate Charge	Q _g	V _{DD} = 15V, I _D = 5A, V _{GS} = 10V	--	14.8	--	nC
Gate-Source Charge	Q _{gs}		--	2.6	--	
Gate-Drain Charge	Q _{gd}		--	2.9	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15V, I _D = 5A, R _G = 3Ω	--	4.5	--	ns
Turn-on Rise Time	t _r		--	2.5	--	
Turn-off Delay Time	t _{d(off)}		--	14.5	--	
Turn-off Fall Time	t _f		--	3.5	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	6.5	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} =5A, V _{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Q _{rr}	I _F = 5A, V _{GS} = 0V di/dt=100A/us	--	56	--	nC
Reverse Recovery Time	T _{rr}		--	47	--	ns

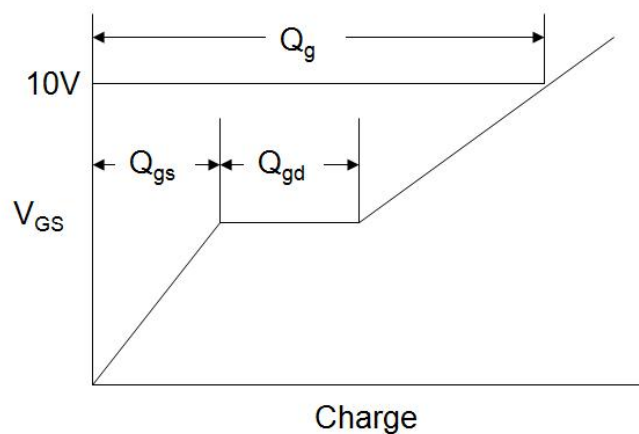
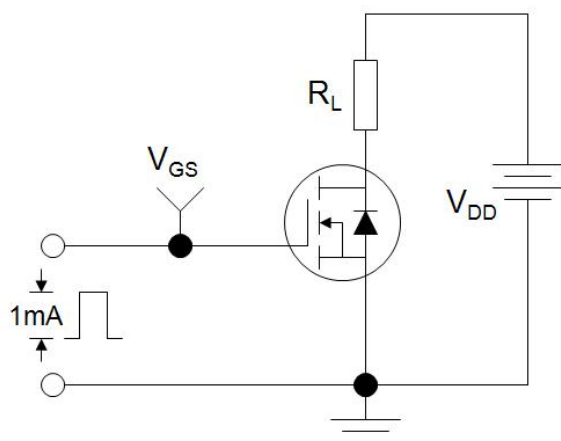
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^\circ\text{C}$, $V_{DD} = 30V$, $V_{GS} = 10V$, $L = 0.5mH$, $R_G = 25\Omega$

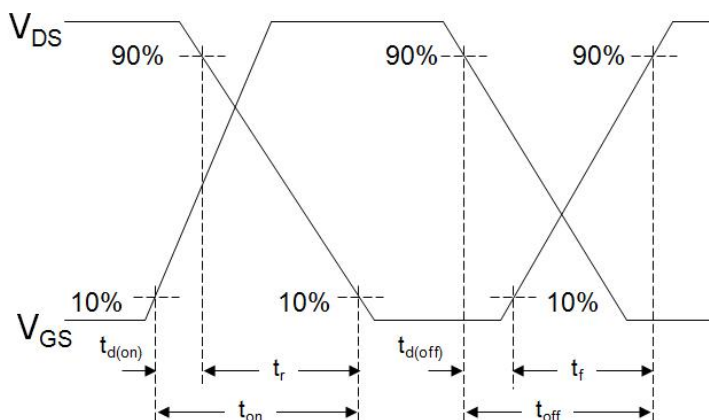
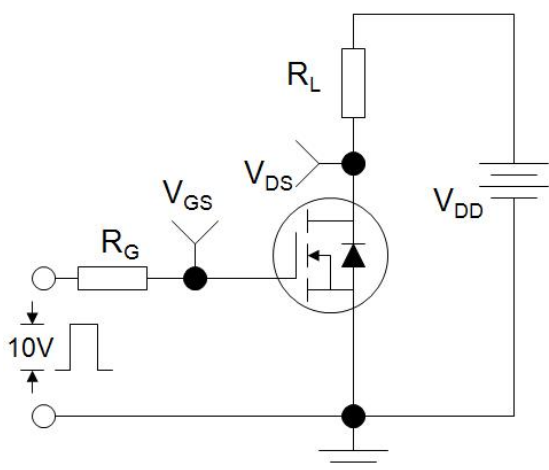
The table shows the minimum avalanche energy, which is 25mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

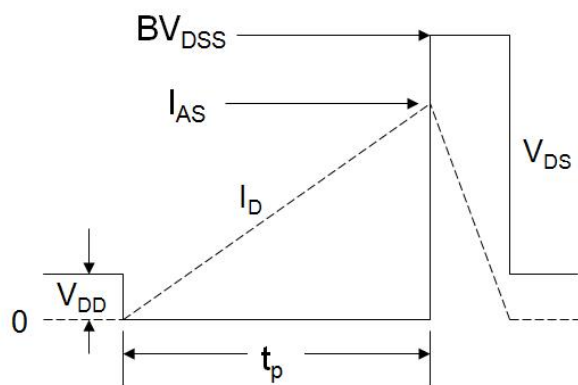
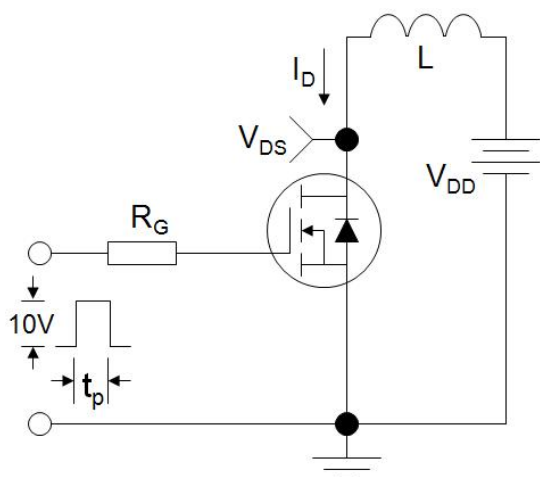
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

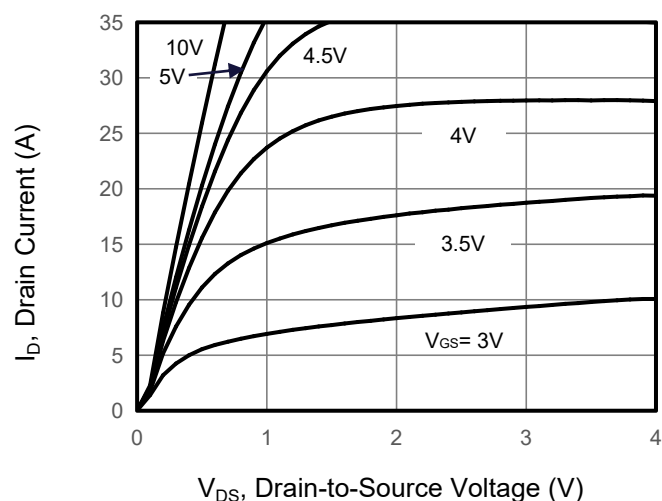


Figure 2. Transfer Characteristics

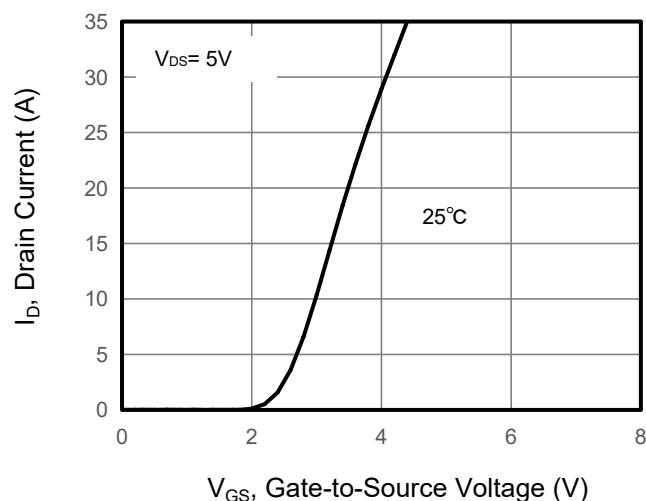


Figure 3. Drain Source On Resistance

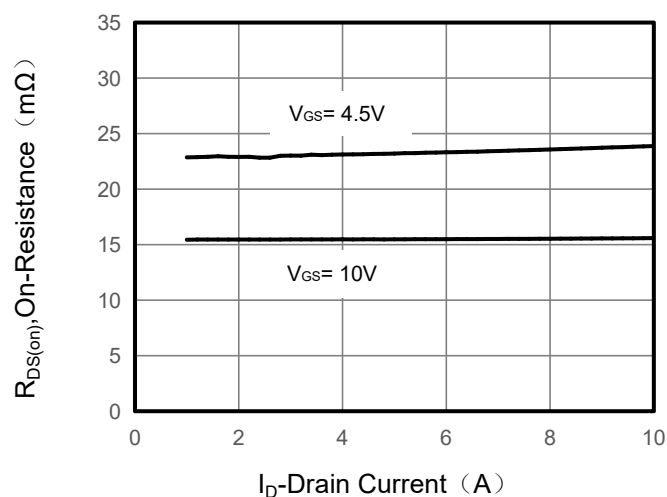


Figure 4. Gate Charge

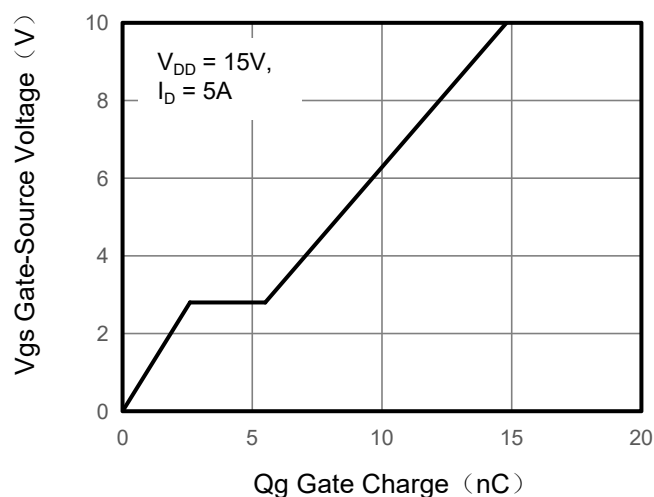


Figure 5. Capacitance

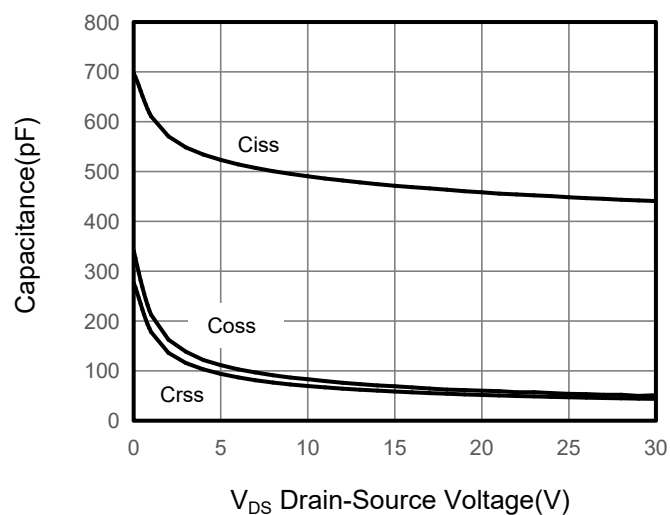
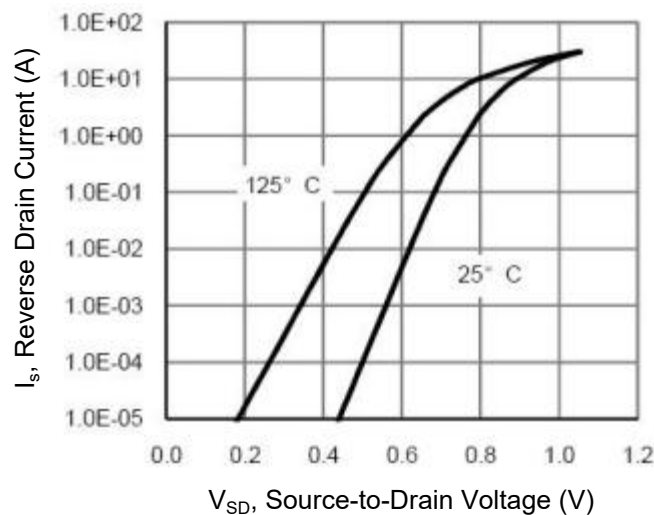


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

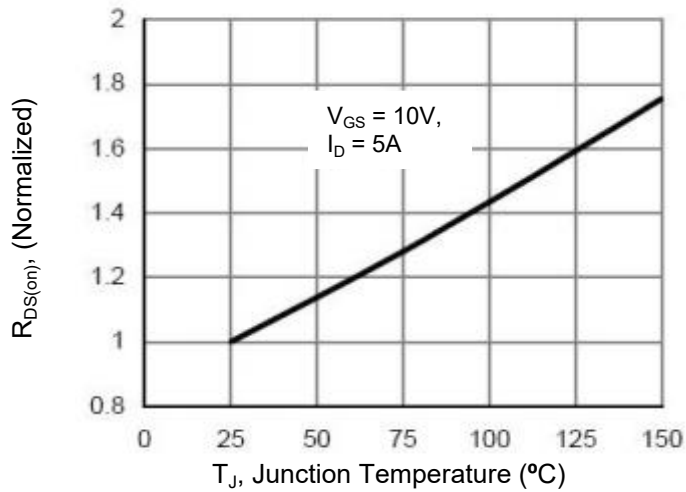


Figure 8. Safe Operation Area

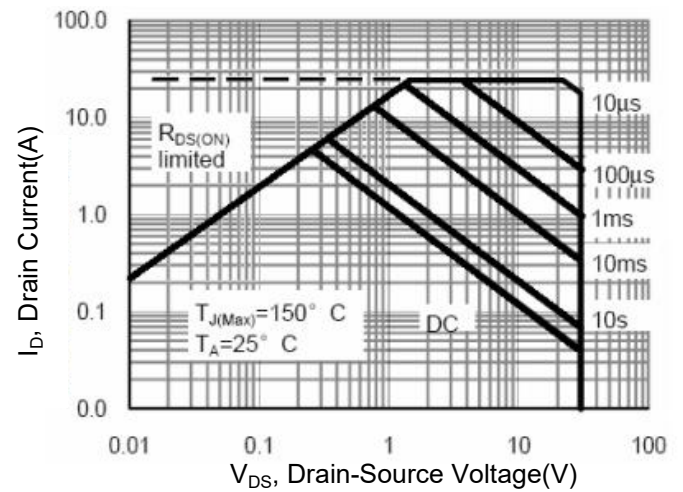
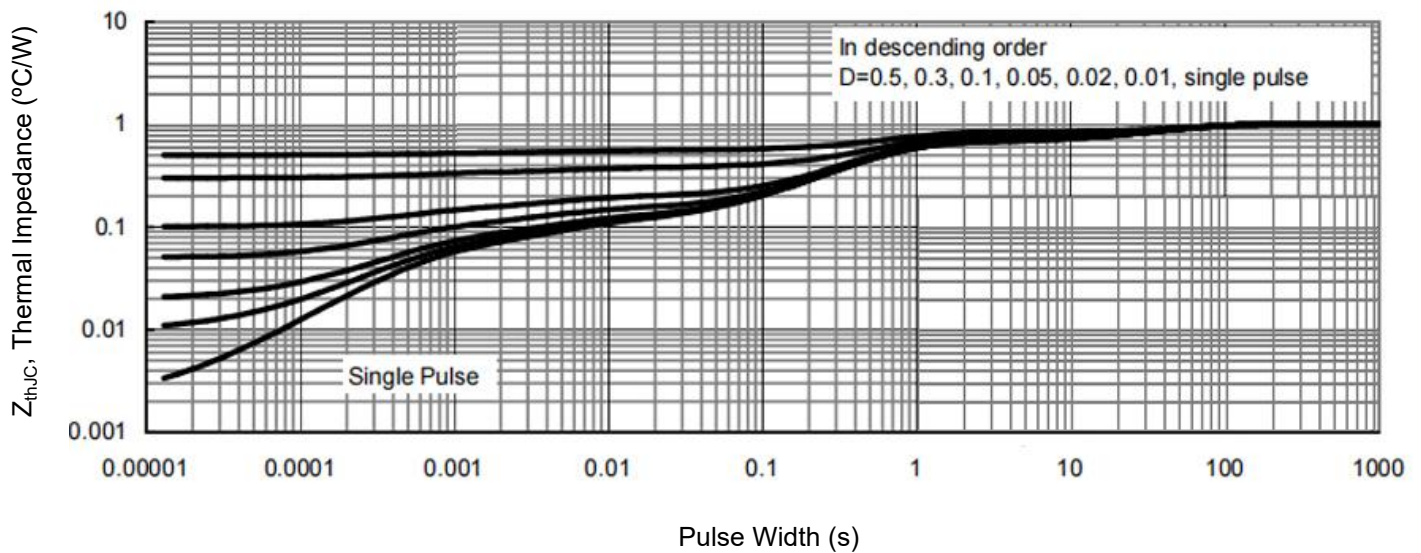


Figure 9. Normalized Maximum Transient Thermal Impedance



PMOS Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30V, V _{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.5	-2.0	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D = -4A	--	37	45	mΩ
		V _{GS} = -4.5V, I _D = -4A	--	57	70	
Forward Transconductance	g _{FS}	V _{DS} = -5V, I _b = -4A	--	8	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz	--	608	--	pF
Output Capacitance	C _{oss}		--	75	--	
Reverse Transfer Capacitance	C _{rss}		--	68	--	
Total Gate Charge	Q _g	V _{DD} = -15V, I _D = -4A, V _{GS} = -10V	--	11	--	nC
Gate-Source Charge	Q _{gs}		--	2	--	
Gate-Drain Charge	Q _{gd}		--	2.6	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = -15V, I _D = -4A, R _G = 3Ω	--	7.5	--	ns
Turn-on Rise Time	t _r		--	5.5	--	
Turn-off Delay Time	t _{d(off)}		--	19	--	
Turn-off Fall Time	t _f		--	7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	-5	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = -4A, V _{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q _{rr}	I _F = -4A, V _{GS} = 0V di/dt=-100A/us	--	66	--	nC
Reverse Recovery Time	T _{rr}		--	53	--	ns

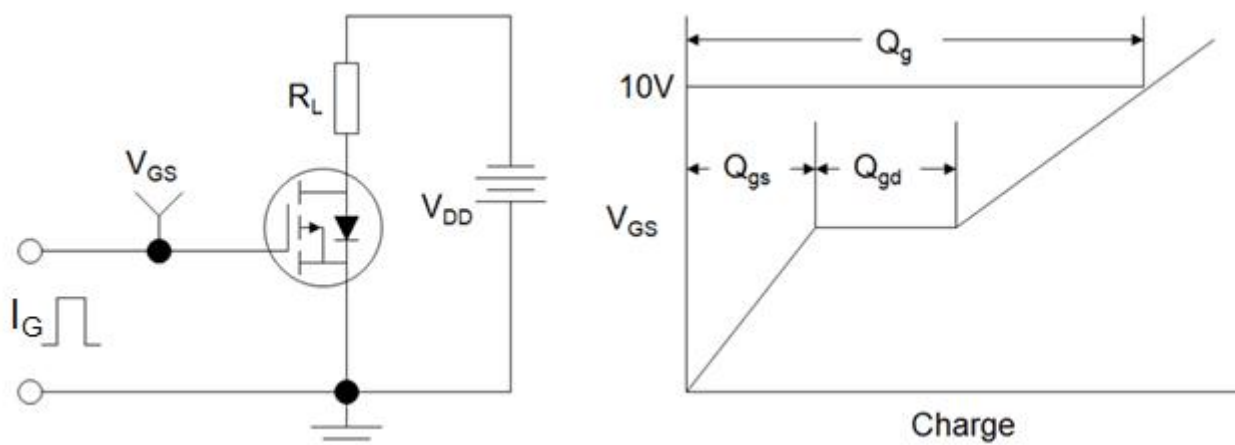
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^\circ\text{C}$, $V_{DD} = -30V$, $V_{GS} = -10V$, $L = 0.5\text{mH}$, $R_G = 25\Omega$

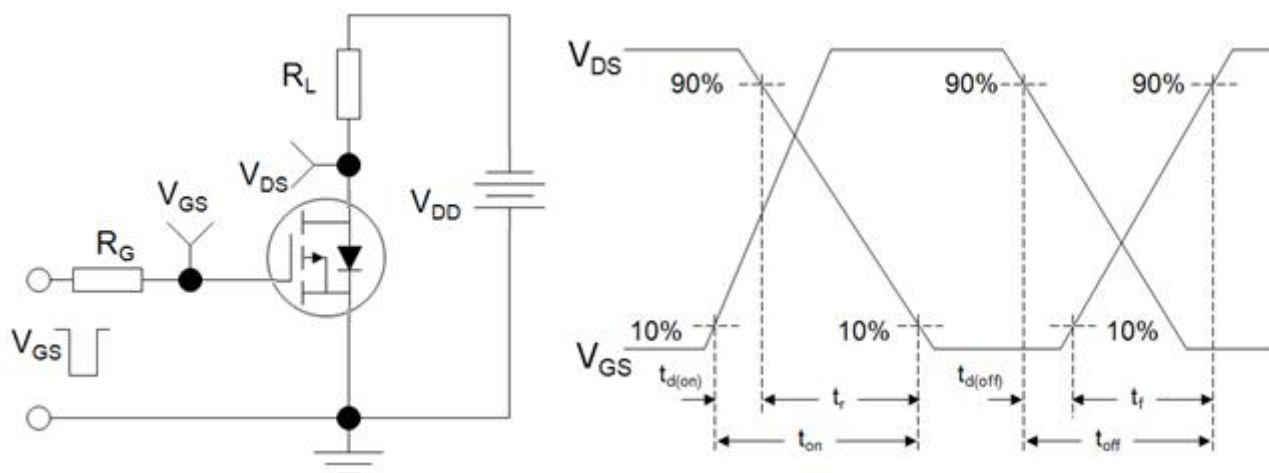
The table shows the minimum avalanche energy, which is 36mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

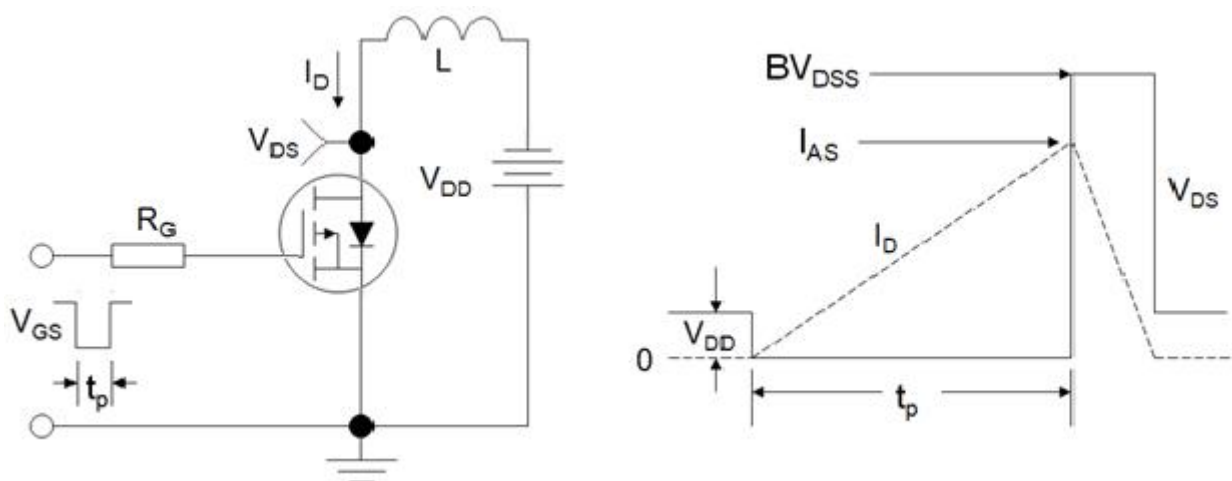
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

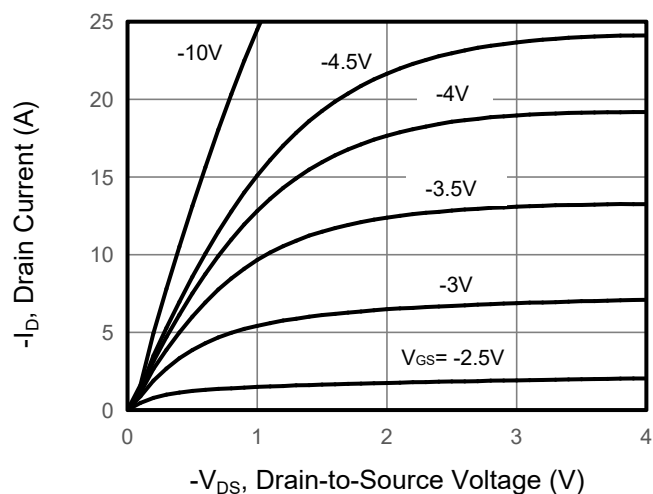


Figure 2. Transfer Characteristics

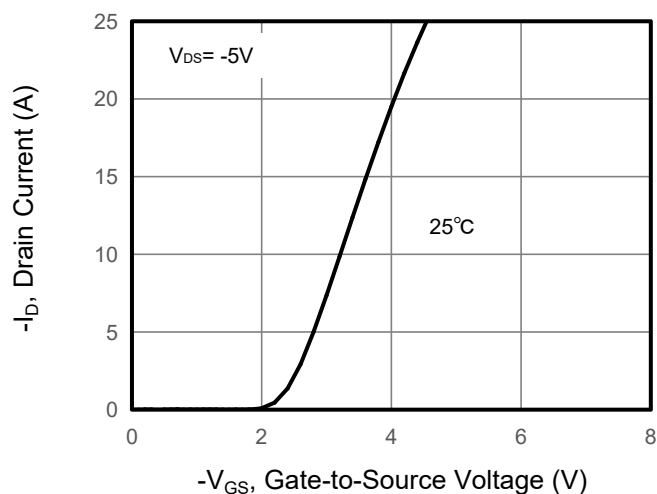


Figure 3. Drain Source On Resistance

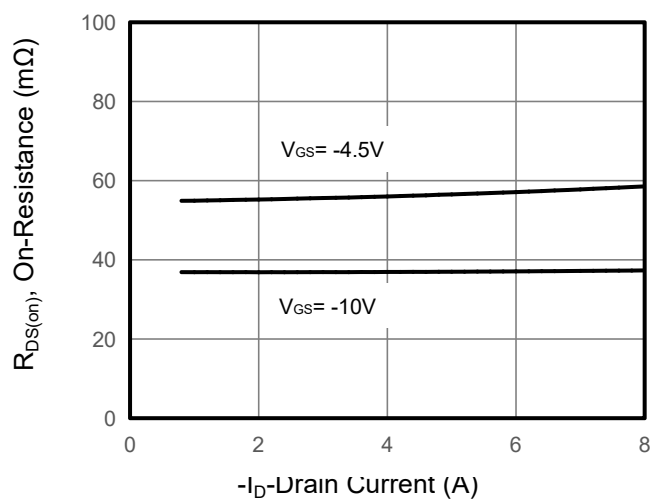


Figure 4. Gate Charge

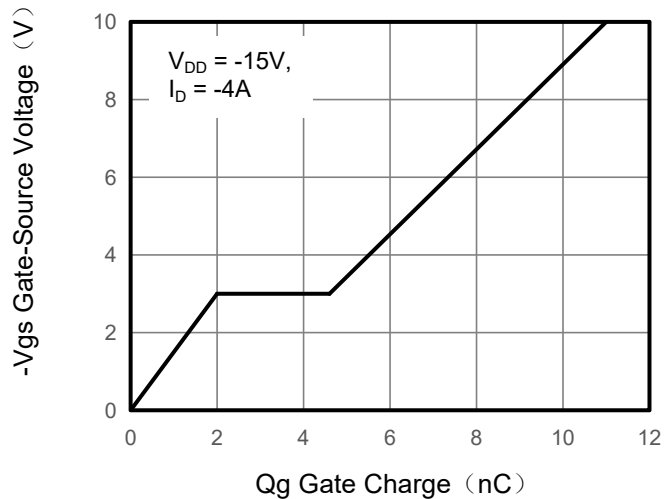


Figure 5. Capacitance

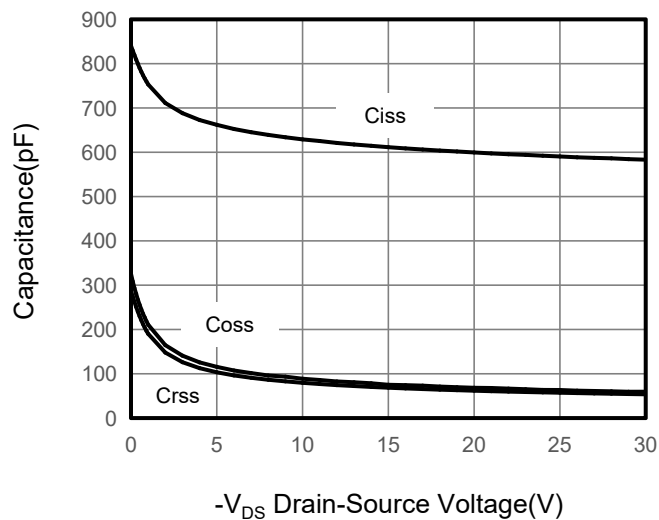
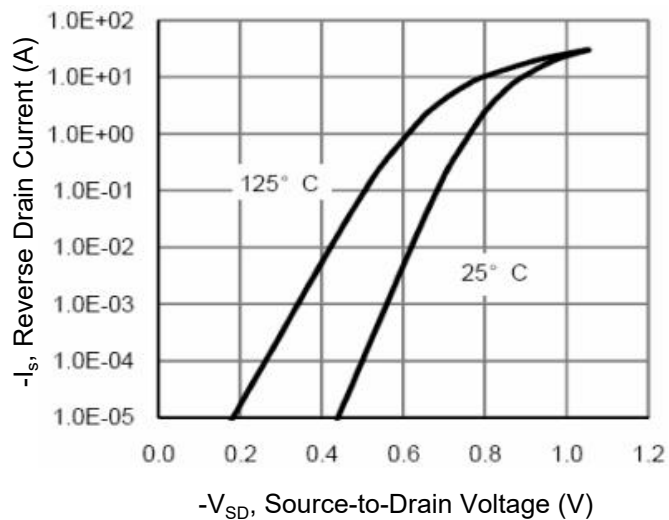


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

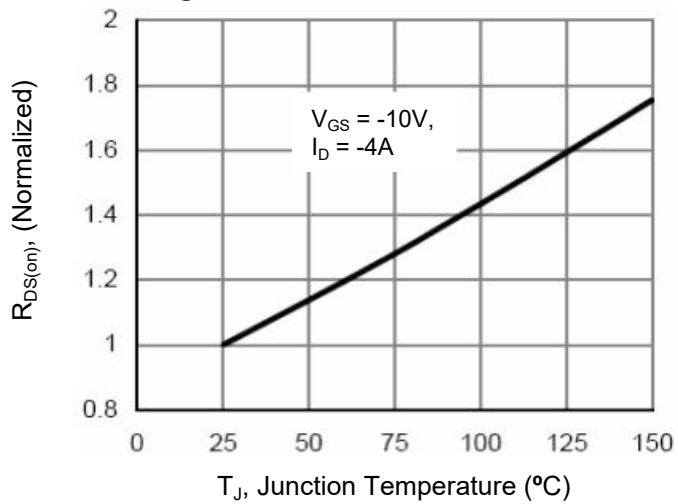


Figure 10. Safe Operation Area

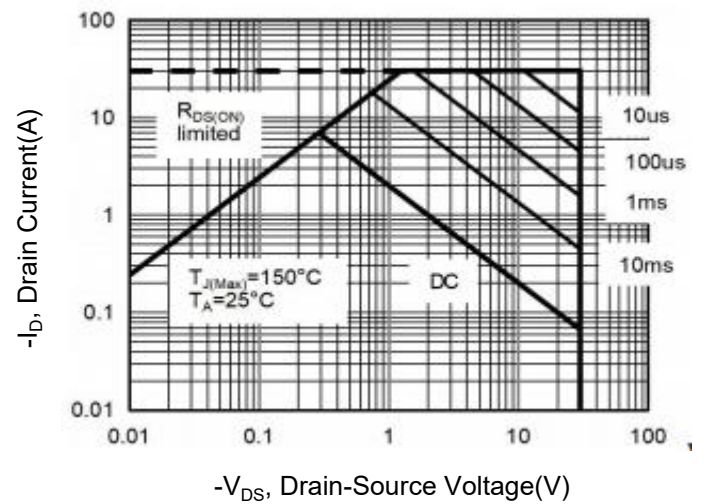
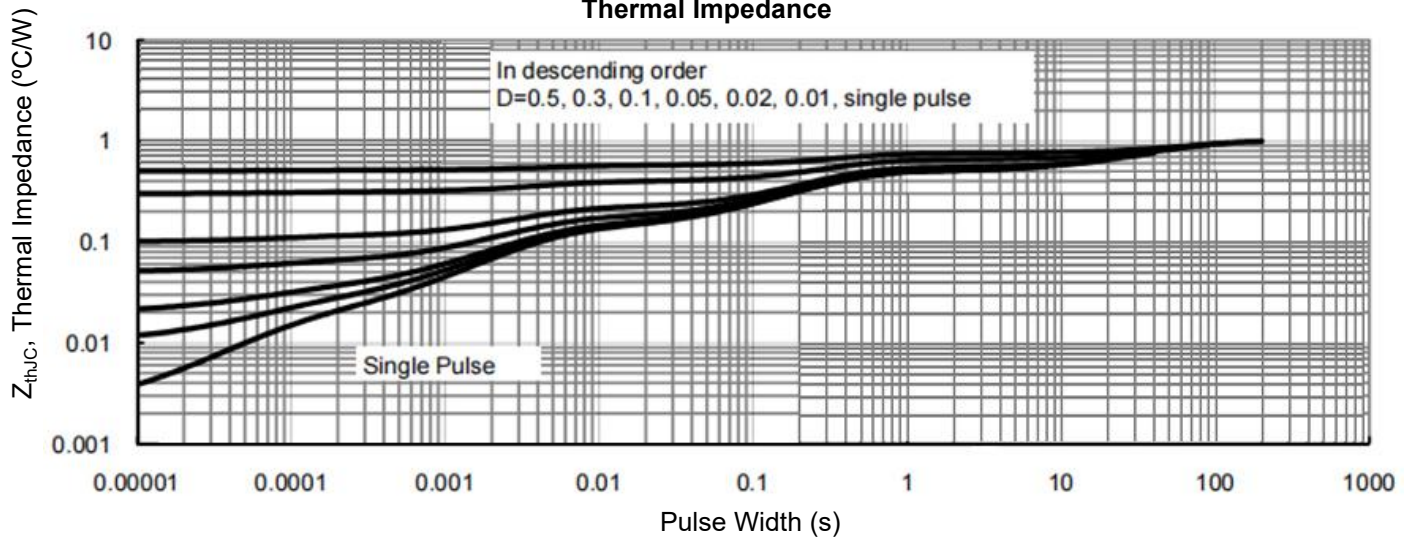


Figure 9. Normalized Maximum Transient Thermal Impedance



SOP-8 Dual Package Information

