CML Microcircuits

COMMUNICATION SEMICONDUCTORS

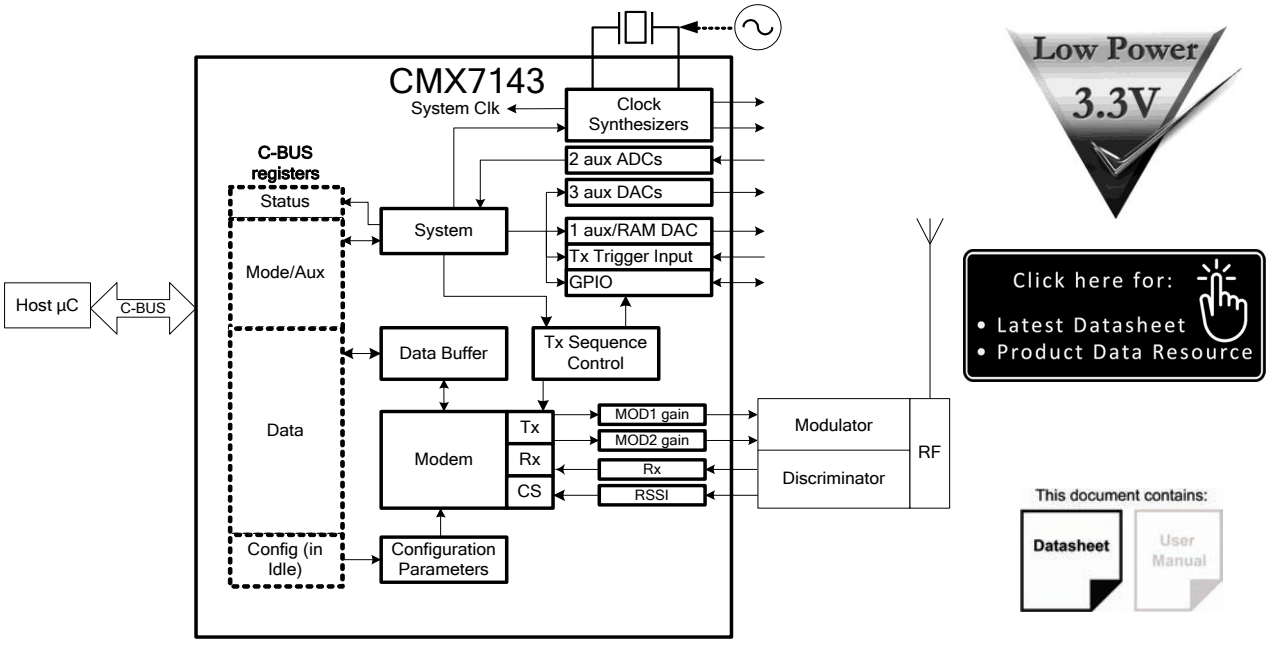
CMX7143
Multi-Mode Wireless Data Modem

D/7143_FI2.0/10 May 2013 **DATASHEET** Provisional Issue

7143FI-2.x 4FSK Packet Data Modem

Features

- **Multiple Modulation Types**
  - **7143 FI-1.0: GMSK/GFSK Modulation**
  - **7143 FI-2.0: 4FSK Modulation -** Over-air compatibility with CMX969 for RD-LAP Tx/Rx
  - **7143 FI-3.0: FFSK/MSK Modulation**
- **Automatic Frame Sync Detection**
- **Automatic Preamble, Frame Sync Insertion**
- **2 x Auxiliary ADCs and 4 x Auxiliary DACs**
- **3 x Analogue Inputs (RSSI or Discriminator)**
- **C-BUS Serial Interface to Host µController**
- **Flexible Bit Rates**
- **Raw Mode, Data Pump, Carrier Sense**
- **Auxiliary System Clock Outputs**
- **Tx Outputs for 2-point or I/Q Modulation**
- **Available in 48-pin LQFP and VQFN Packages**
- **Low-power 3.3V Operation**
- **Flexible Powersave Modes**
- **Formatted or Raw Data Modes**
- **Soft Decision Data Bits**



1 Brief Description

Designed for use in wireless data modems, the CMX7143 with 7143FI-2.x is a half-duplex modem with carrier sense and automatic control of transmit hardware, including a RAMDAC for PA ramping. Carrier sense provides a listen before talk capability, automatically reverting to receive if activity on channel is detected. In receive, automatic frame sync detection provides acquisition of the received signal with minimal host intervention. Two different frame sync patterns may be searched for concurrently, with little need for preamble.

Continued...

Other features include two Auxiliary ADC channels with four selectable inputs and up to four auxiliary DAC outputs (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

Coded mode supports block types compatible with the CMX919 and CMX969 (RD-LAP) modems.

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or from a host µController over the built-in C-BUS serial interface. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 7143FI-2.x. Separate Function Images™ are available which support GFSK/GMSK and FFSK/MSK modulation.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in this product with your local CML representative.

CONTENTS

Table Page

Figure Page

It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
10	• Added RD-LAP channel coding block types in FI-2.x.	15.5.13
9	• Clarification of BOOTEN options by Table 1 and Table 4. • Correction of error in Figure 6.	26.7.11
8	• Clarification of P4.x program block nomenclature and minor typographical errors. Clarification of maximum bit/byte counter value in raw mode (TxData 0 and RxData 0). Definition of the action of any unused bits added. Default pre-amble length in P0.8 corrected to 18 symbols.	01.12.09
7	• Additional information about CRC2 Reset, Insert Preamble, insert FS1 and insert FS2 features added in 7143FI-2.1.2.0. • Clarification of additional delay required when preloading data in Tx Idle or CS Idle modes, in section 7.4.14, and additional delays for all consecutive C-BUS writes.	06.10.09
6	• Changes to Pin names, Register and Bit names for consistency with other FIs. *(Functionality is unchanged, but drawings, tables and text descriptions updated).* • Addition of a “Last tail” status bit in Tx for 7143FI-2.1.1.0. Description added. • Table in section 11.1 replaced by a hyperlinked register table. • Descriptions of the b15..12 allocation in section 11.2.4 corrected. • Definition of maximum signal levels clarified. • Details of Fine output attenuation in Program Blocks P4.9 and P4.10 added. • FI loading procedure, P3.x tables and Reset mechanisms clarified. • Style of EDS changed to conform to latest guidelines, logos, etc. also updated. • Document is now "Provisional Issue".	31.07.09
5	• Changes to Program Block P4.1 specification to allow for selection of Tx RRC+Sinc and an Rx RRC+Inverse Sinc filter OR RRC for both Tx and Rx. • Changes to Program Block P4.1 specification to allow for selection of soft bit outputs in raw mode. • Changes to the description of RxData registers and RxControl register to define soft output operation. • Error in power up bit specification corrected (Power Down Control register). • Added explanation of RSSI and inverted P4.7 and P4.8 in Program Blocks. • Minor typographical corrections.	04.02.09
4	• Correction in rates that the host should read/write Aux Data Control registers. • Correction to time units used to specify Carrier Sense/Tx Sequence. • Added reference to "CMX7143 Modem Performance" App. Note.	17.06.08
3	• Add operating current in ‘DC Parameters’. • Remove DC blocking capacitors from signal inputs (figure 2). • Editorial formatting of AV_{DD} in P1.2 default values and other minor typographical corrections. • Clarification of which bits are used in raw and formatted modes in register $C3. • Correction of description of b5 in $C6 concerning RxData0 ($B8) and TxData0 ($B5). • Section 11.1, $C6, b1 corrected to ‘X’.	13.05.08

2	• Added P3.7 parameter to select 10 sample per symbol mode (7143FI-2.0.1.0 and later). • Added P4.6 parameter description true for (7143FI-2.0.1.0 and later). • Updates of package diagrams. • Correction to content of Program Block P3.3 – add 128. • Added late trans bit (7143FI-2.0.1.0 and later). • Added section on data preload (7143FI-2.0.1.0 and later). • Corrected some missing status bits in the summary table. • Correction to spec of registers $A9, $CD. • General updating typos/editorial terms to match 7143FI-1.x documentation. • Correct references to P3.3, each needs 128 subtracting from it. • Addition of I/Q mode modulation spectra and other diagrams.	08.01.08
1	• Original document, prepared for first beta release of software.	05.09.07

2 Block Diagram

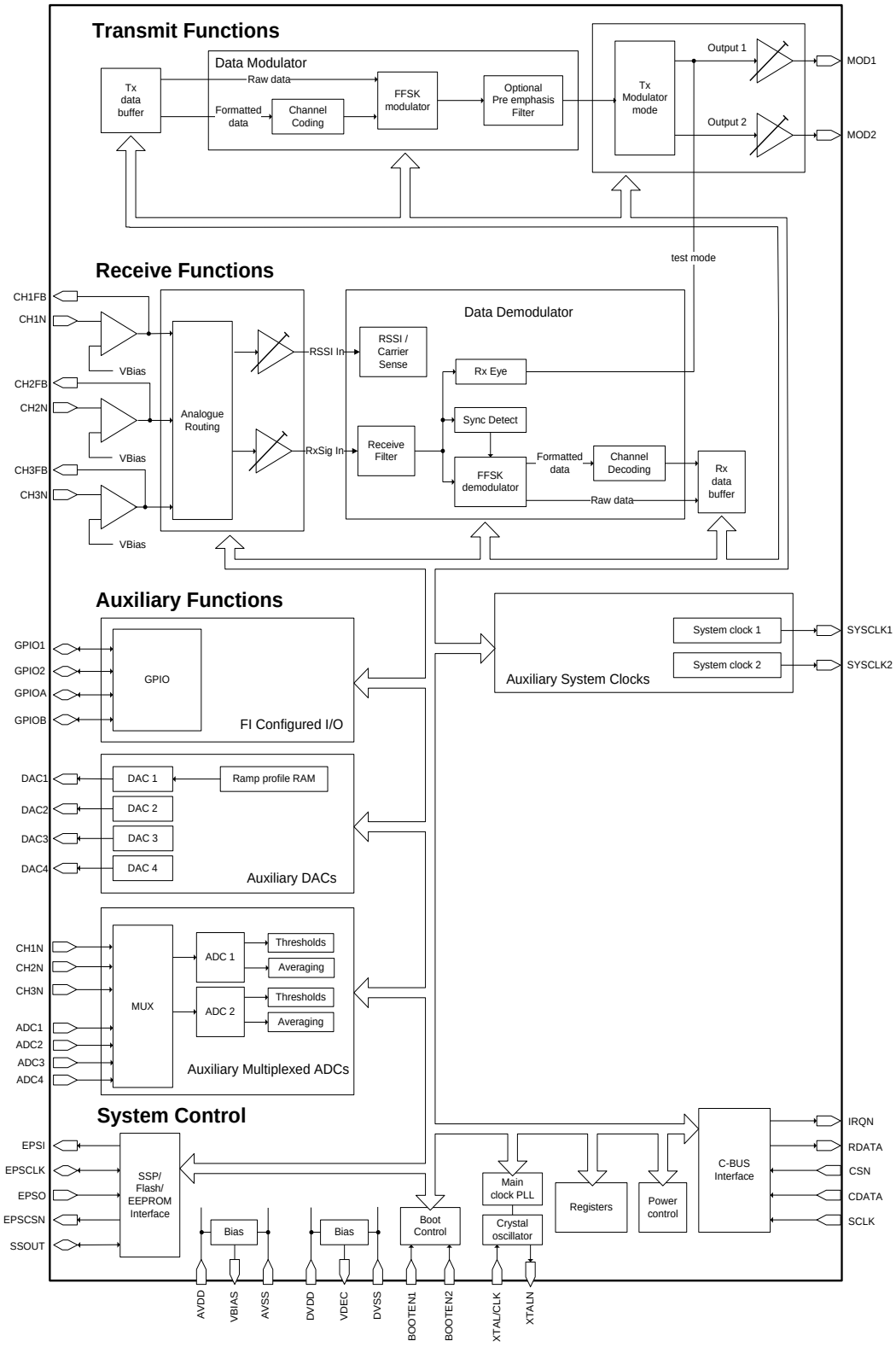


Figure 1 Block Diagram

3 Signal List

CMX7143 48-pin Q3/L4	Pin Name	Type	Description
1	EPSI	OP	SPI bus Master Output
2	EPSCLK	BI	SPI bus Serial Clock
3	EPSO	IP+PD	SPI bus Master Input
4	EPSCSN	OP	Flash/EEPROM Chip Select
5	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
6	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
7	DVSS	PWR	Digital Ground
8	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
9	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.
10	GPIO1	BI	General Purpose I/O pin
11	GPIOA	BI	General Purpose I/O pin
12	GPIOB	BI	General Purpose I/O pin
13	SYSCLK1	OP	Synthesized Digital System Clock Output 1
14	DVSS	PWR	Digital Ground
15	GPIO2	BI	General Purpose I/O pin
16	CH1N	IP	Channel 1 inverting input for RxSig/RSSI
17	CH1FB	OP	Channel 1 input amplifier feedback
18	CH2N	IP	Channel 2 inverting input for RxSig/RSSI
19	CH2FB	OP	Channel 2 input amplifier feedback
20	CH3FB	OP	Channel 3 input amplifier feedback
21	CH3N	IP	Channel 3 inverting input for RxSig/RSSI
22	AVSS	PWR	Analog Ground
23	MOD1	OP	Modulator 1 output
24	MOD2	OP	Modulator 2 output
25	VBIAS	OP	Internally generated bias voltage of approximately $AV_{DD}/2$, except when the device is in 'Powersave' mode when VBIAS will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.
26	Reserved	NC	No connection should be made to this pin
27	ADC1	IP	Auxiliary ADC input 1
28	ADC2	IP	Auxiliary ADC input 2

CMX7143 48-pin Q3/L4	Pin Name	Type	Description
29	ADC3	IP	Auxiliary ADC input 3
30	ADC4	IP	Auxiliary ADC input 4
31	AVDD	PWR	Analog +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
32	DAC1	OP	Auxiliary DAC output 1/RAMDAC
33	DAC2	OP	Auxiliary DAC output 2
34	AVSS	PWR	Analog Ground
35	DAC3	OP	Auxiliary DAC output 3
36	DAC4	OP	Auxiliary DAC output 4
37	DVSS	PWR	Digital Ground
38	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.
39	XTAL/CLK	IP	input from the external clock source or Xtal
40	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external Clock used.
41	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.
42	CDATA	IP	C-BUS: Serial data input from the µC
43	RDATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
44	SSOUT	BI	SPI bus Chip Select
45	DVSS	PWR	Digital Ground
46	SCLK	IP	C-BUS: The C-BUS serial clock input from the µC
47	SYSCLK2	OP	Synthesized Digital System Clock Output 2
48	CSN	IP	C-BUS: The C-BUS chip select input from the µC
EXPOSED METAL PAD	SUB	-	On this device, the central metal pad (which is exposed on Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AV_{ss}). **No other electrical connection is permitted.**

Notes:
IP = Input (+ PU/PD = internal pull-up/pull-down resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

4 External Components

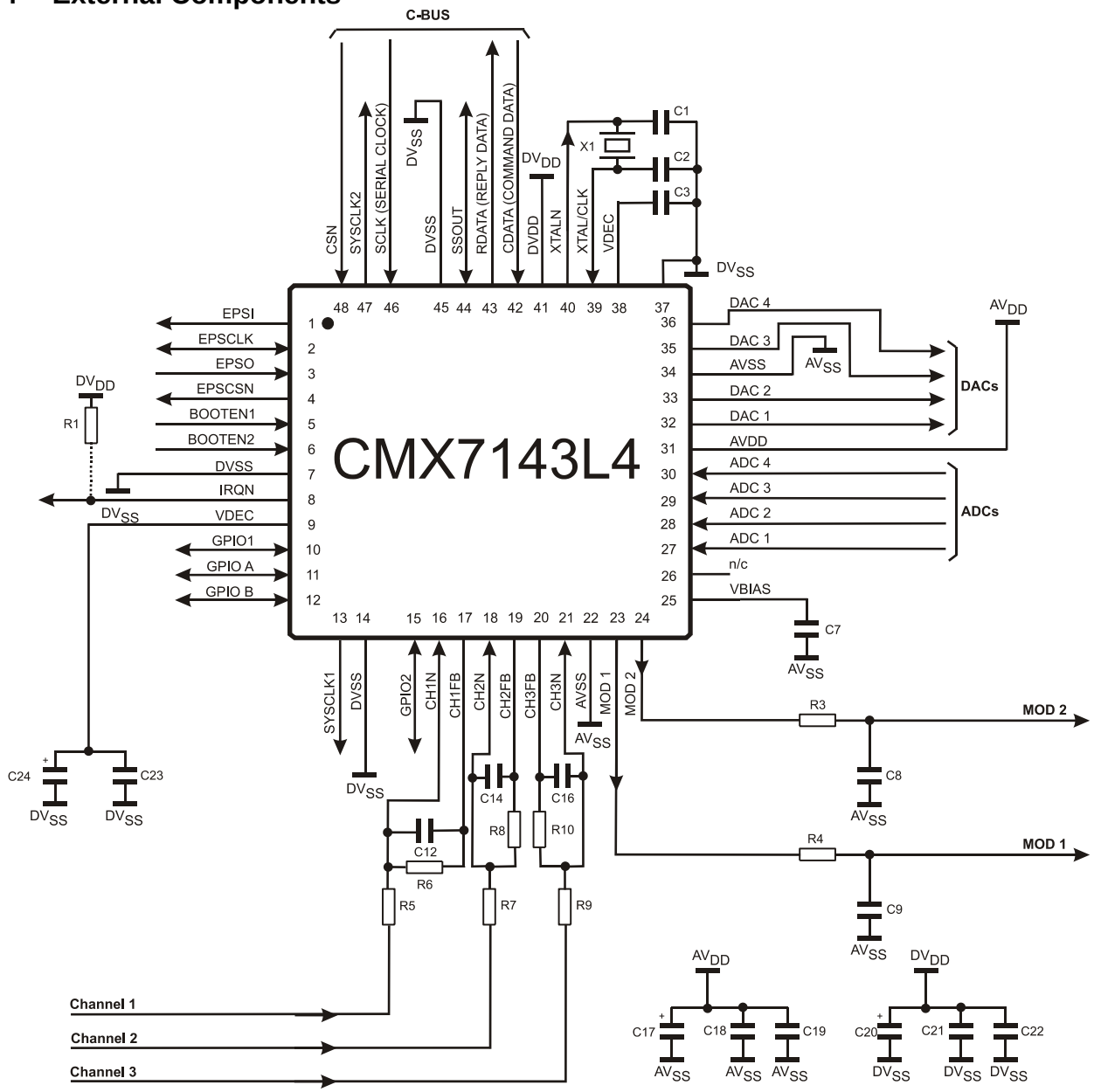


Figure 2 CMX7143 Recommended External Components

R1	100kΩ	C1	18pF			C21	10nF
		C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF			C23	10nF
R4	100kΩ			C14	100pF	C24	10µF
R5	See note 2	C5	N/F				
R6	100kΩ	C6	N/F	C16	200pF		
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	9.6 or 19.2MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ			C20	10µF		

Resistors ± 5%, capacitors and inductors ± 20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 9.6MHz crystal or 19.2MHz external oscillator is assumed, other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain of the first discriminator/RSSI input, as follows:

$$|GAIN_1| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the CH1FB pin is within the discriminator input signal range specified in 7.6.2.

3. R7 should be selected to provide the desired dc gain of the second discriminator/RSSI input as follows:

$$|GAIN_2| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the CH2FB pin is within the discriminator input signal range specified in 7.6.2.

4. R9 should be selected to provide the desired dc gain of the third discriminator/RSSI input, as follows:

$$|GAIN_3| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the CH3FB pin is within the discriminator input signal range specified in 7.6.2.

5. If any of the Channel inputs are not required, the respective pin should be connected to AV_{SS}.

6. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both V_{DEC} pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each V_{DEC} pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both V_{DEC} pins.

5 PCB Layout Guidelines and Power Supply Decoupling

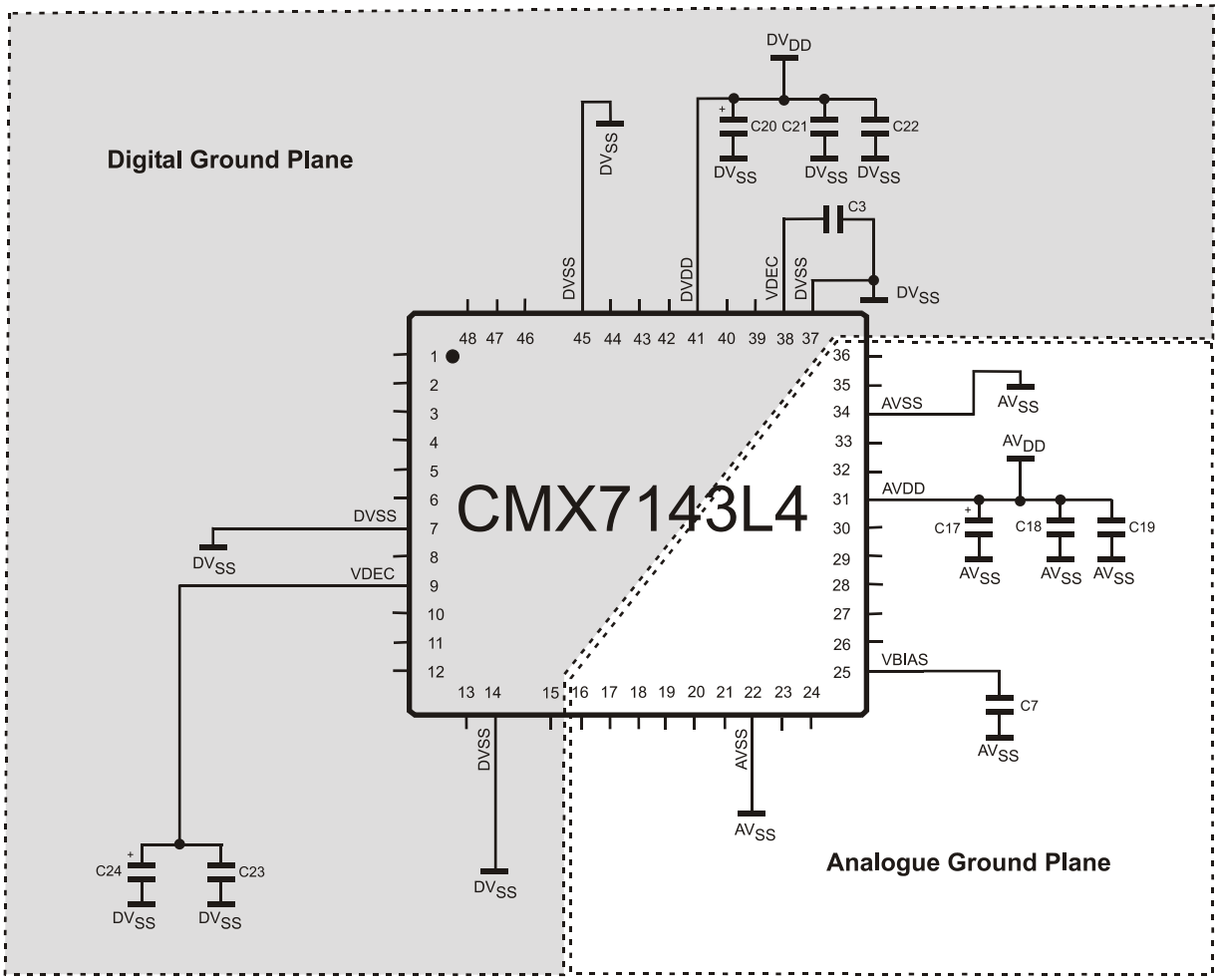


Figure 3 CMX7143 Power Supply and De-coupling

Component Values as per Figure 2.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7143 and the supply and bias decoupling capacitors. The decoupling capacitors C3, C7, C18, C19, C21, C22, and C23 should be as close as possible to the CMX7143. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7143, with provision to make links between them, close to the CMX7143. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the de-coupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The crystal, X1, may be replaced with an external clock source.

6 General Description

6.1 CMX7143 Features

The CMX7143 is intended for use in half-duplex modems. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required.

A block diagram of the device is shown in Figure 1.

Inputs to the RxSig and RSSI/CS signal processing blocks of the Data Demodulator can be routed from any of the three channel input pins (CH1N, CH2N or CH3N).

Tx Functions:

- Flexible Tx data transfer block size, up to 104bits
- Automatic preamble, frame sync insertion simplifies host control
- Modulator producing 2-point or I/Q outputs with programmable deviation
- Data pulse shape filtering
- RAMDAC capability for PA ramping control
- Tx trigger feature allowing precise control of burst start time
- Tx burst sequence for automatic RAMDAC ramp and Tx hardware switching
- Carrier sense for “listen before talk” operation
- Raw and Formatted (Channel coded) data modes

Rx Functions:

- Demodulator input with input amplifier and programmable gain adjustment
- Flexible Rx data transfer block size, up to 104bits
- Automatic frame sync detection simplifies host control
- Rx filtering
- Tracking of symbol timing and received signal levels
- Raw and Formatted (Channel coded) data modes

Auxiliary Functions:

- 2 programmable system clock outputs
- 2 auxiliary ADCs with four selectable input paths
- 4 auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- Four GPIO pins
- Tx trigger input (Provided by GPIO1)
- Flash/EEPROM boot mode
- C-BUS (host) boot mode

While in Idle mode, the AuxADC can be used to detect the RSSI signal from the RF section, while still retaining a significant degree of power saving within the CMX7143 and obviating the need to wake the host up unnecessarily. The use of the programmable thresholds allows for user selection of wake-up threshold programmed from the host.

In Carrier Sense mode, RSSI will be sampled using the selected RxSig/RSSI input and averaged automatically by the CMX7143, resulting in a decision to transmit or not based on the presence of a signal on the channel.

Both transmit and receive data can be raw or in the form of coded data blocks. Coding is compatible with the FX919B and MX919B.

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX7143 is designed to work with a Xtal with a frequency of 9.6MHz, or an external frequency oscillator of 9.6 or 19.2MHz. Program Block 3 (see User Manual) must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of configuration values can be found in Table 5 supporting baud rates of 2k to 10k symbols per second (4k to 20kbps). Rates other than those tabulated (within this range) may be possible. Further information can be provided on request.

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7143 and the host µC; this interface is compatible with Microwire™, SPI™[1] and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see Interrupt Operation.

7.2.1 C-BUS Operation

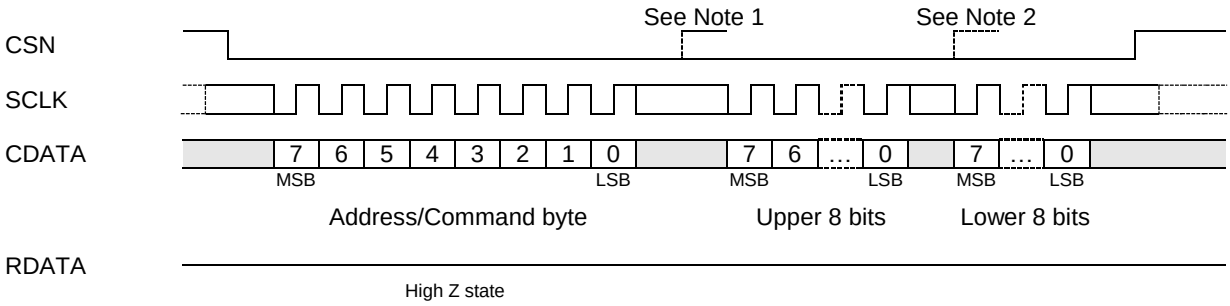
This block provides the transfer of data, control and status information between the CMX7143's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC. This may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX7143's write only Registers, or one or more data byte(s) read out from one of the CMX7143's read only Registers, as illustrated in Figure 4.

Data sent from the µC on the CDATA line is clocked into the CMX7143 on the rising edge of the SCLK input. RDATA from the CMX7143 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

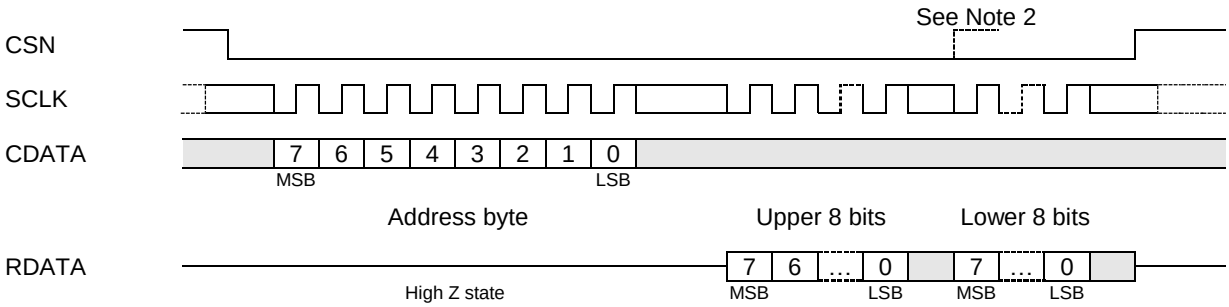
The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 9.2. Note that, due to internal timing constraints, there must be an appropriate delay between subsequent writes to the same C-BUS register. This delay allows for C-BUS polling and is 3 x AuxClk periods for mode changes and 1 x AuxClk period for all other writes. See section 7.4.15.

[1] Microwire™ is a trademark of National Semiconductors, SPI™ is a trademark of Motorola

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 4 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external EEPROM or Flash memory. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7143 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 220k resistor (see Table 1).

For Flash/EEPROM load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the EEPROM or Flash memory in-situ from the host, either a jumper to DV_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Table 1).

Once the FI has been loaded, the CMX7143 performs these actions:-

(1) The product identification code ($7143) is reported in C-BUS register $C5
(2) The FI version code is reported in C-BUS register $C9
(3) The two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) The device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) Once activated, the device initialises fully, enters Idle mode and becomes ready for use.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power cycled before an attempt is made to re-load the FI and re-activate..

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 1 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
Serial Memory load	0	1
No FI load	0	0

Note: Following a General reset, reloading of the Function Image is strongly recommended.

7.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7143 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7143 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7143.

If the host detects a brownout, the BOOTEN state should be set to re-load the FI. A General Reset should then be issued and the appropriate FI load procedure followed.

Each time the Programming register, $C8, is written, it is necessary to wait for the PRG flag (Status register ($C6) b0) to go high before another write to $C8. The PRG flag going high confirms the write to

the Programming register has been accepted. The PRG flag state can be determined by polling the Status register or by unmasking the interrupt (Interrupt Mask register, $CE, b0).

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

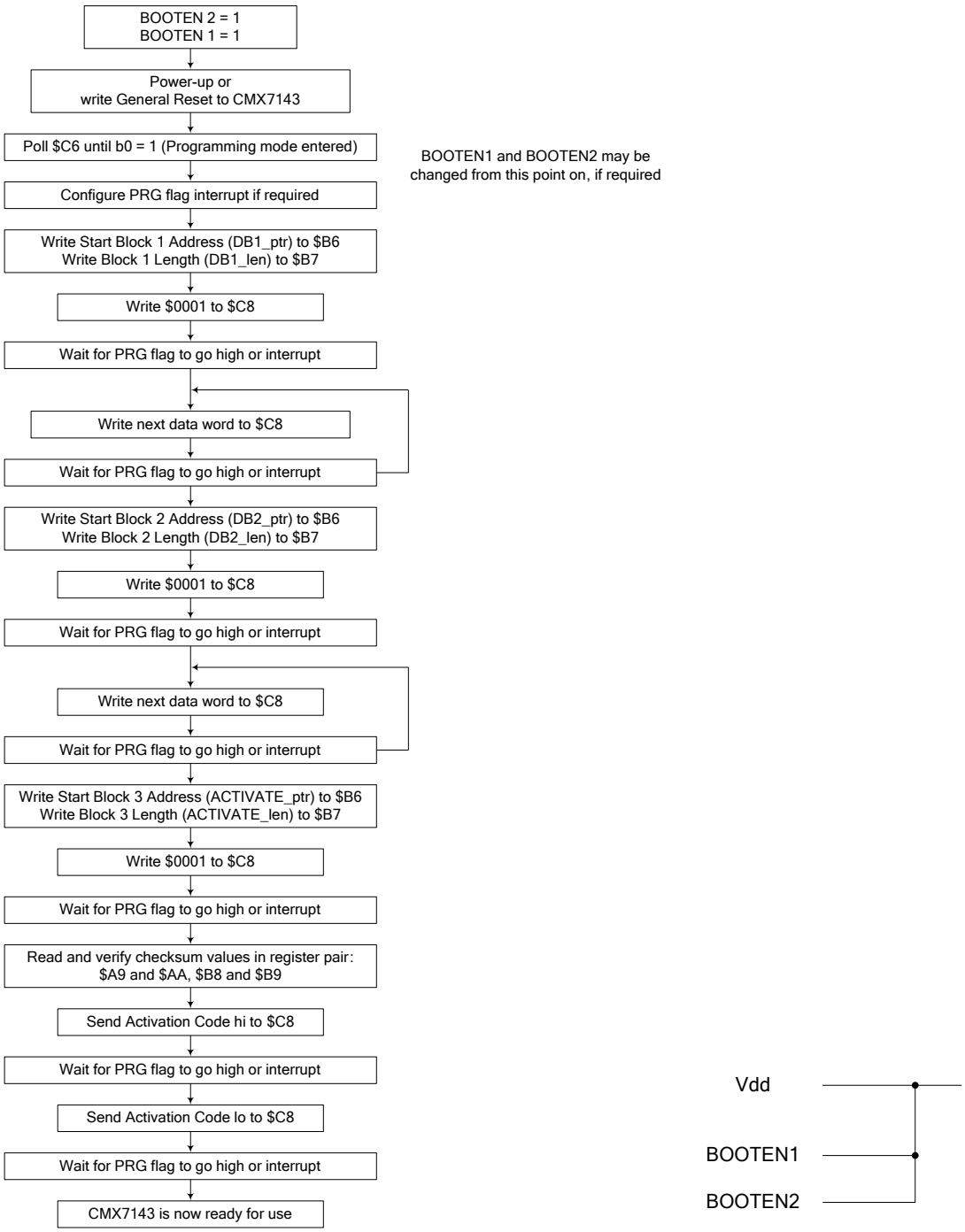


Figure 5 FI Loading from Host

7.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the Flash/EEPROM programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The CMX7143 needs to have the BOOTEN pins set to serial memory load, and then on power-on, or following a C-BUS General Reset, the CMX7143 will automatically load the data from the serial memory without intervention from the host controller.

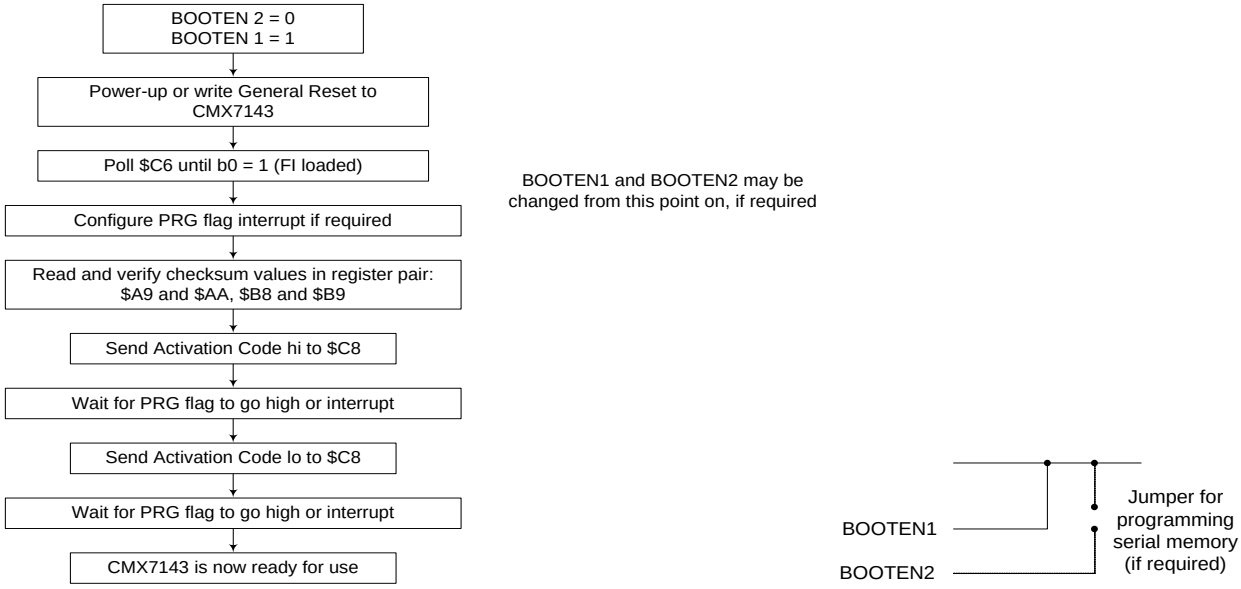


Figure 6 FI Loading from Serial Memory

The CMX7143 has been designed to function with Atmel AT25HP512 serial EEPROM and the AT25F512 Flash EEPROM devices[2], however other manufacturers parts may also be suitable. The time taken to load the FI is dependant on the Xtal frequency, with a 9.6MHz Xtal, it should load in less than 1 second.

[2] Note that these two devices have slightly different addressing schemes. 7143FI-2.x is compatible with both schemes, whereas previous FI 's were only compatible with the AT25HP512 addressing scheme.

7.4 Device Control

Once the Function Image is loaded the CMX7143 can be set into one of four main modes using the Modem Mode and Control - $C1 write register:

- Idle mode – for configuration or low power operation
- Transmit mode – for transmission of raw or formatted data
- Receive mode – for detection and reception of bursts containing raw or formatted data
- Carrier Sense mode – for attempting to transmit if the channel is free, otherwise continuing to receive

These four modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers in Transmit, Receive and Carrier Sense modes or, for parameters that are not likely to change during operation, using the Programming register ($C8) in Idle mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. Additional power-saving can be achieved by disabling the unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- Power Down Control - $C0 write
- Modem Mode and Control - $C1 write
- Programming Register – $C8 write

7.4.1 Normal Operation Overview

In normal operation (after the CMX7143 is configured) the appropriate mode must be selected and data provided in transmit or retrieved in receive. This process is carried out by selecting the mode (Tx, Rx or Carrier Sense), Frame Sync 1 or 2 and formatted or raw data. Such a selection is required at the beginning of transmission or reception of a burst.

In transmit (or following a carrier sense period where no signal is detected on channel) the CMX7143 will begin by switching GPIO signals as configured by the transmit sequence. The RAMDAC can also be configured to ramp up at this point. Transmission then begins with preamble and the selected frame sync. The main payload of user data comes next, ending with selectable tail bits. The burst ends with the transmission sequence ramping the RAMDAC down and/or switching GPIO signals.

In receive (or following a carrier sense period where signal is detected on channel) the CMX7143 will begin by searching for either or both of the configured frame sync patterns. On detection of a frame sync, reception and data output will begin. Reception continues until the CMX7143 is switched into a different mode, determined by the host.

During the burst, data blocks must be transferred into or out of the CMX7143. Each of these transfers uses the RxData or TxData registers to transfer data and the Status register to indicate that the data has been dealt with successfully. Each transfer can contain a host selectable number of bits or bytes. The CMX7143 can be configured to interrupt the host on completion of a data transfer.

The CMX7143 offers internal buffering of data in addition to the RxData and TxData registers in both receive and transmit directions. The amount of buffering offered is dependant on the mode in which the device is operating and the size of any transfers carried out by the host. In the process of burst transmission or reception the most significant registers are:

- Modem Mode and Control - $C1 write
- Status - $C6 read
- Interrupt Mask - $CE write
- RxControl - $C3 write
- TxData0 - $B5 write (Plus TxData1-6)
- RxData0 - $B8 read (Plus RxData1-6)

7.4.2 Device Configuration (Using the Programming register)

While in Idle mode the Programming register becomes active. The Programming register provides access to the Program Blocks. Program Blocks allow configuration of the CMX7143 during major mode change. Features that can be configured include:

- Flexible selection of Baud rates, from 2k to 10k baud.
- Pre-amble and frame syncs to be using in transmit and receive
- Selection of Automatic control of 4 x GPIO and the RAMDAC during transmission
- Configuration of RAMDAC profile
- Configuration of AuxADC and RSSI averaging
- Programming of input and output gains and offsets
- Configuration of the carrier sense window and thresholds

Full details of how to configure these aspects of device operation are given in section 10.2 in the User Manual.

7.4.3 Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration outside of Idle mode. Configuration of the following features is possible:

- Auxiliary ADC detect thresholds
- Auxiliary ADC input selection and averaging mode
- Power down control
- Input gain and input/output signal routing

The registers that allow configuration of these features are:

- AuxConfig - $A7 write
- AuxConfig2 - $CD write
- Power Down Control - $C0 write
- Input Gain and Input/Output Signal Routing - $B1 write

7.4.4 Interrupt Operation

The CMX7143 can produce an interrupt output when various events occur. Possible events include detection of a frame sync, an overflow of the internal data buffering in receive, or completion of transmission whilst in transmit.

Each event has an associated Status register bit and an Interrupt Mask register bit. The Interrupt Mask register is used to select which status events will trigger an interrupt on the IRQN line. All events can be masked using the IRQ mask bit (bit 15) or individually masked using the Interrupt Mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the Status register reflects the IRQN line state.

All interrupt flag bits in the Status register, except the PRG flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. See:

- Status - $C6 read
- Interrupt Mask - $CE write

7.4.5 Signal Routing

The CMX7143 offers a flexible routing architecture, with three signal inputs and two modulator outputs. The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the Program Blocks.

One of the three input sources (CH1N, CH2N or CH3N) should be routed to RxSig In and another to RSSI In. Output1 and Ouput2 should be routed to MOD1 and MOD2, as required.

The input source routed to RxSig In will be treated as the input signal to demodulate. This is expected to be the demod output from a limiter discriminator.

The input source routed to RSSI In will be averaged and the result presented in the Aux Data Registers. If carrier sense is selected then the same input source will be averaged over a short period internally in order to make the decision on whether to transmit or not.

The output signals MOD1 and MOD2 will provide 2-point modulation outputs with independently programmable gains. Alternatively, an I/Q output may be selected, in which case MOD1 and MOD2 will provide in phase and quadrature signals.

See:

- Input Gain and Input/Output Signal Routing - $B1 write
- AuxConfig2 - $CD write

7.4.6 Tx Mode

In typical Tx operation, the preamble and FS1 or FS2 are transmitted automatically (default values may be changed by use of the Program Blocks), and then data from the TxData Block is transmitted directly until the mode is changed to Rx or Idle. The first block of data MUST be loaded into the TxData registers BEFORE executing the modem mode change to Tx.

The host should write the initial data to the C-BUS TxData registers and then set modem control to the required transmit type with the Mode bits as Tx. As soon as the data has been read from the C-BUS TxData registers the DataRDY IRQ will be asserted (when configured correctly). More data should be loaded into the TxData registers at this stage before data buffered in the CMX7143 runs out, otherwise the burst will end.

For precise control of the instant that transmission starts it is possible to trigger a transmission using GPIO1 as an input. In addition to triggering the modulation output, it is possible to define a transmission sequence with defined RAMDAC ramp up/down, and GPIO on/off events. The transmission sequence is configured using Program Block 1. Selecting a Tx mode with GPIO1 configured as an “automatic input” places the device into a “Tx pending” state, where it is neither receiving nor transmitting, just waiting for a trigger on GPIO1 to begin transmission.

In general Figure 7 can be extended to represent operation when a transmit sequence is defined by the host by:

- Removing the need for the host to provide a ramp up – instead the configured Tx sequence will deal with this.
- Inserting GPIO on/off events before ramp up and after ramp down as specified by the transmit sequence.

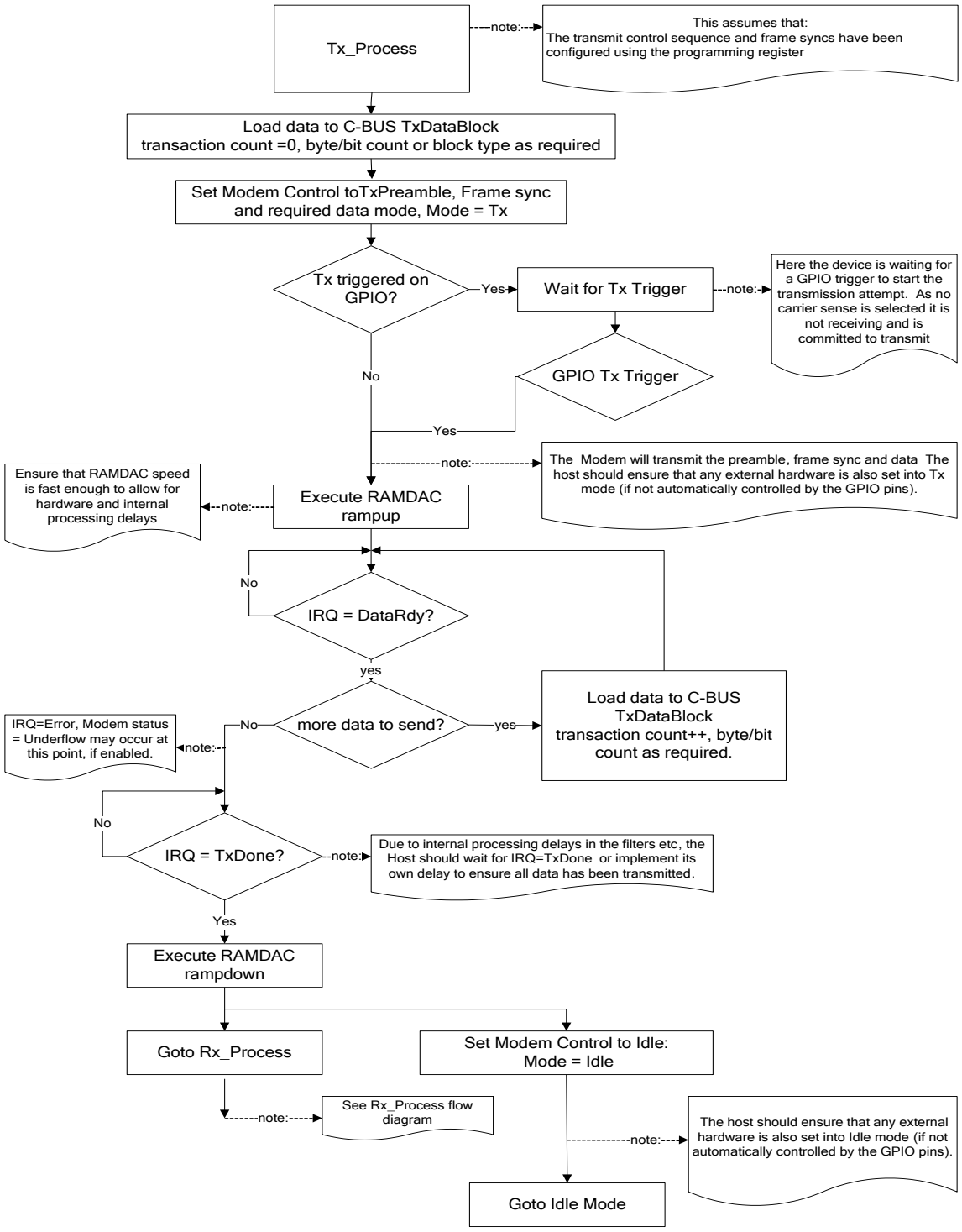


Figure 7 Host Tx Data Flow (No Tx sequence/Carrier sense)

7.4.7 Rx Mode

In Rx mode a frame sync must be detected, then data is supplied to the host through the RxData registers and should be read in response to a DataRDY IRQ (when configured). The CMX7143 will continue decoding the input waveform until the host sets the Mode bits to either Tx or Idle, as required. A test mode to examine the Rx "EYE" is also provided.

Once initial timing is established, timing corrections can be derived from the data to track the received signal. The Modem control register allows selection of the tracking mode used to track both the signal level and symbol timing of the input signal. It is recommended that the automatic modes are used.

If the UseTrans bit in the RxControl register is set to 0 the device will update the C-BUS RxData registers with payload data as it becomes available and the host MUST respond to the DataRDY IRQ before the data is over-written by the modem. If UseTrans is set to 1 then the host can use the transaction counter in the RxControl register to control the data read transaction rate.

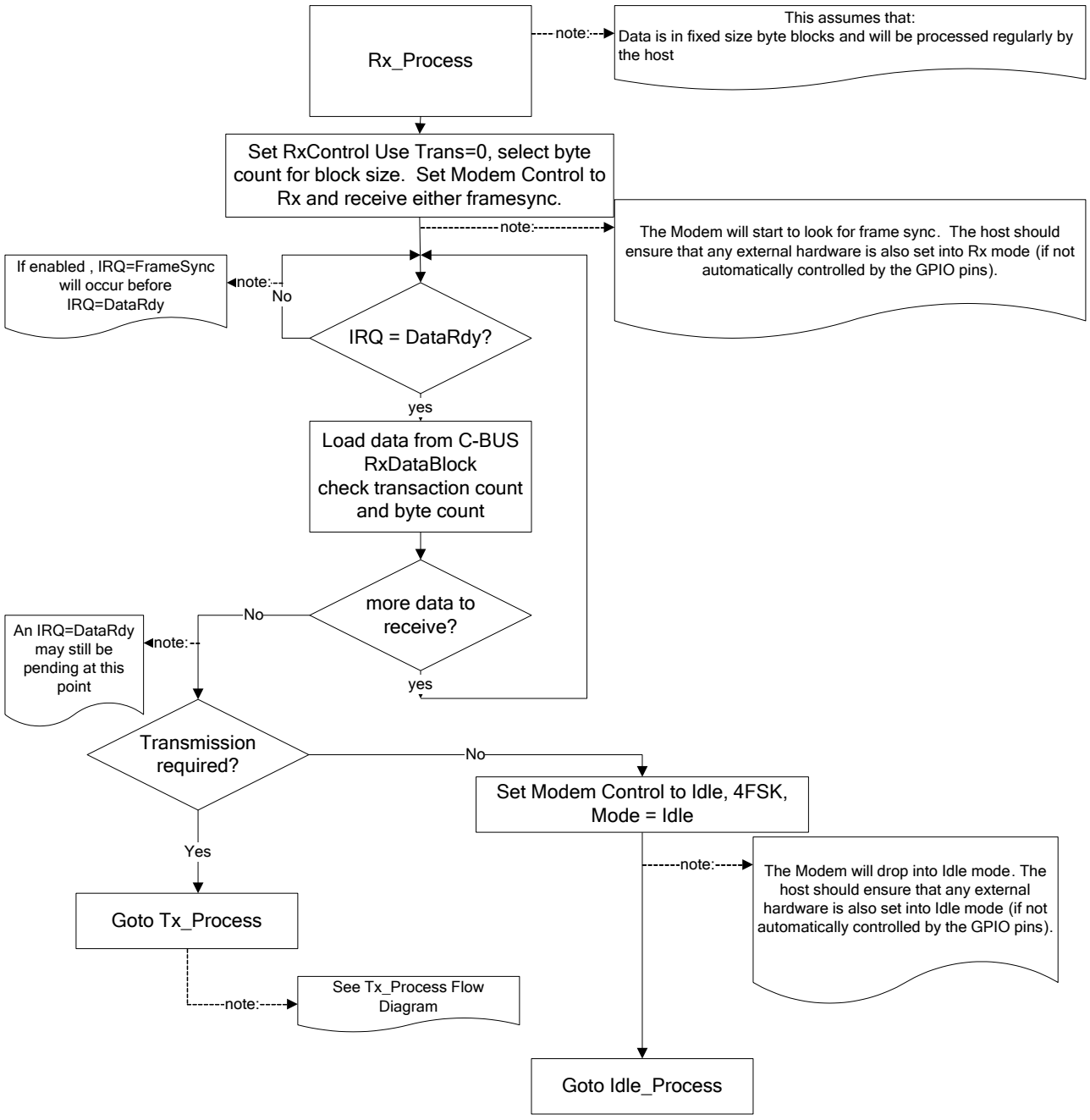


Figure 8 Host Rx Data Flow (Use Trans=0)

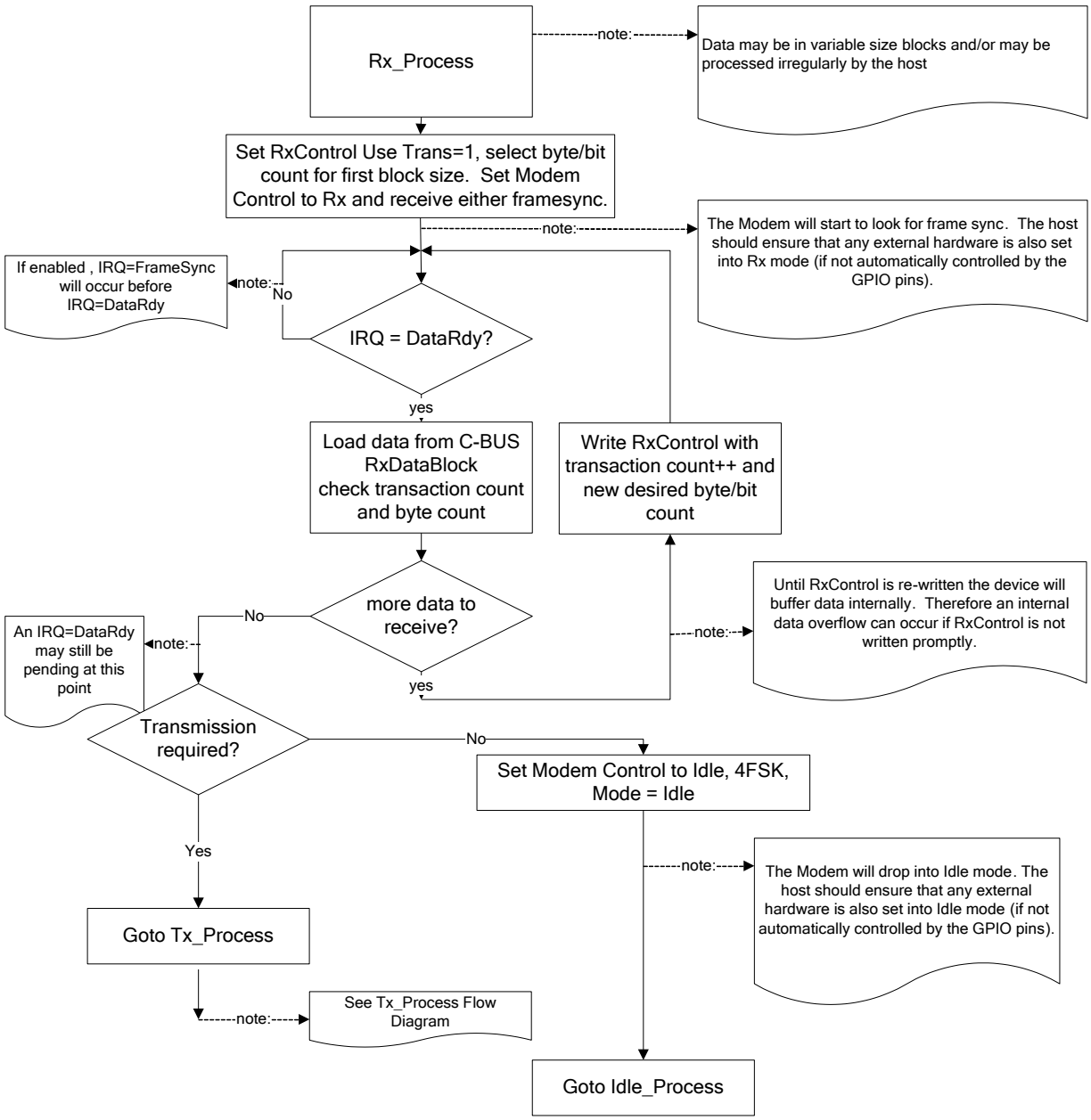


Figure 9 Host Rx Data Flow (Flow controlled data with UseTrans=1)

7.4.8 Carrier Sense Mode

Carrier Sense mode is a receive mode, pending a transmission. A carrier sense period, averaging window length and threshold must be defined in the Program Blocks prior to entering this mode. For this mode to operate correctly an RSSI signal must be connected to the RSSI/carrier sense input.

On entry to Carrier Sense mode reception will begin (or continue if the previous mode was receive) with an attempt to search for a frame sync. During the defined carrier sense period average RSSI will be computed over a moving window. Three outcomes are possible:

1. If during the carrier sense period the average RSSI is above the carrier sense threshold then transmission will be aborted, and search for frame sync will continue. The device reverts to receive.
2. There is a possibility that a valid frame sync will be detected during the carrier sense period. If this is the case, the transmission will be aborted immediately and the device reverts to receive.
3. If the RSSI average remains below the carrier sense threshold then transmission will proceed.

In each of the three possible cases, status bits will be used to indicate the result of the carrier sense period.

If the carrier sense mechanism is used in conjunction with GPIO1 as a Tx trigger operation is as follows: The device is put in receive, searching for a frame sync. If frame sync is found during this period then it is indicated to the host via the status bits and normal reception resumes. No carrier sense happens until GPIO1 is used to start the transmit process, at which point carrier sense begins and operation is as described above.

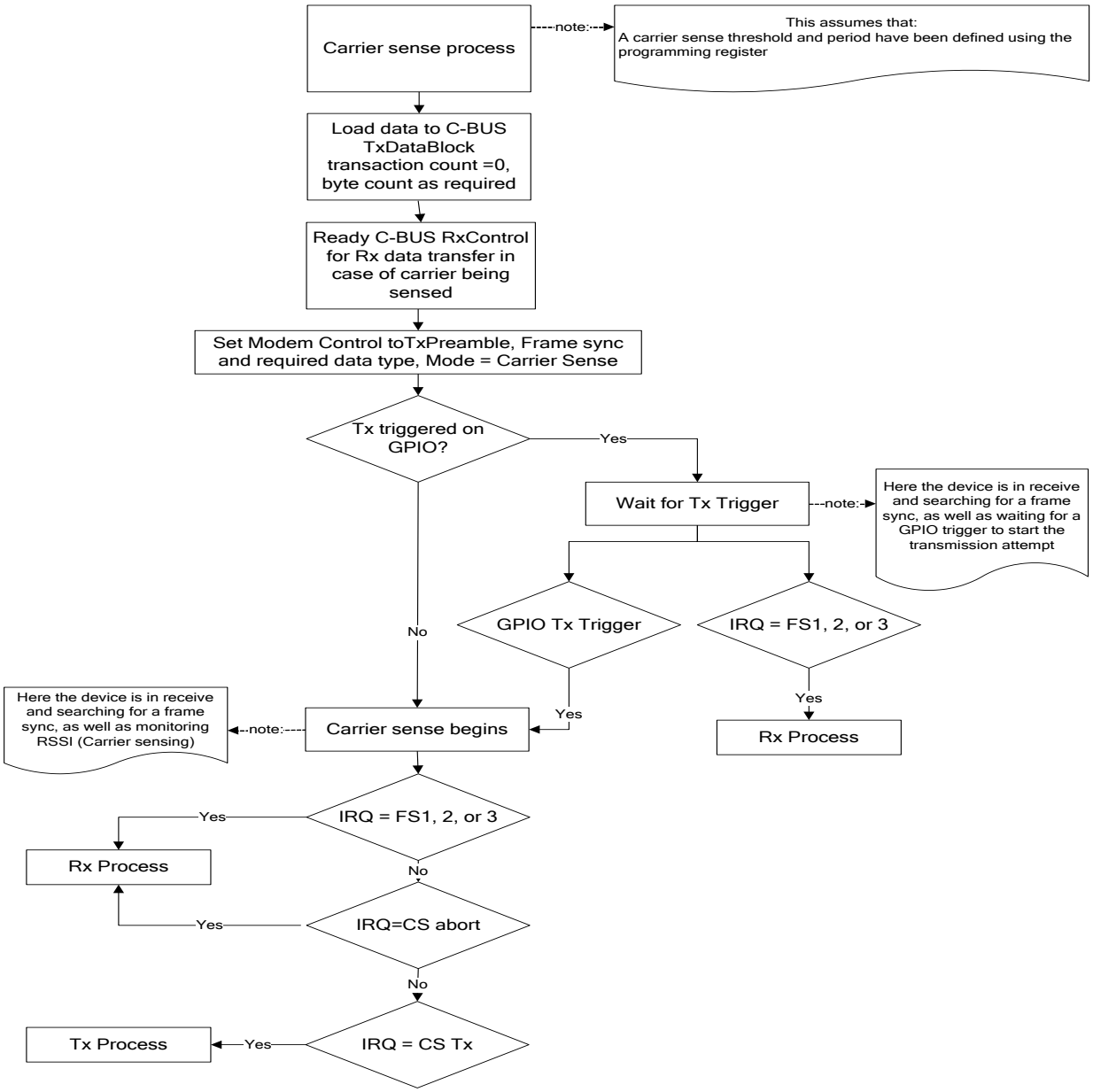


Figure 10 Carrier Sense

7.4.9 The Transmit Sequence

The CMX7143 is capable of being configured to provide the following features:

1. Selecting Tx mode results in transmission beginning directly on entry to Tx mode or is delayed until GPIO1 is used as an input trigger.
2. Selecting Carrier Sense mode will result in behaviour as in point 1, followed by a carrier sense period, where transmission is delayed (reception continues) until a carrier sense period is completed and no activity is sensed on the channel.
3. Once started, transmission can be configured to be a simple modulation output or can include a programmable sequence of events including RAMDAC rampup/down and GPIO On/Off.

   Each of these 3 options can be selected independently of the others. The following diagram illustrates transmit operation.

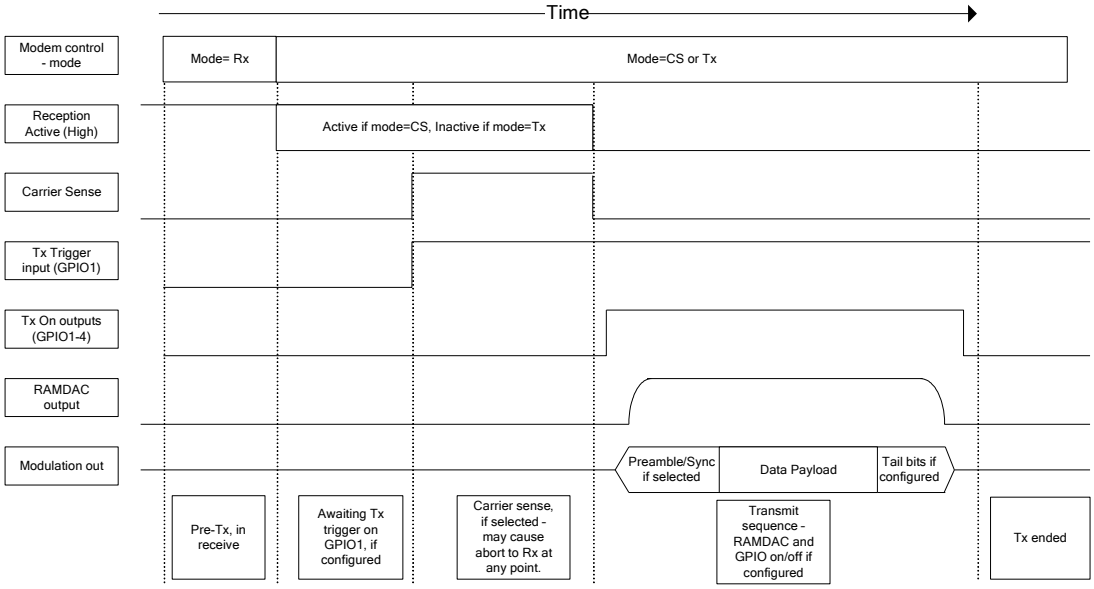


Figure 11 Transmit Sequence

7.4.10 Other Modem Modes

In Rx mode, it is possible to output the received signal as an “EYE” diagram for test and alignment purposes. In this configuration, the filtered received signal is presented at the MOD1 pin and a trigger pulse at the MOD2 pin (derived directly from the XTAL/CLK source) to allow viewing on a suitable oscilloscope. In some cases it is advisable to obtain a trigger pulse that is synchronised to the transmitting modem symbol rate.

In Tx mode, a fixed PRBS sequence or a fixed preamble transmission is provided which can be used for test and alignment.

7.4.11 Data Transfer

The payload data is transferred to and from the host via a block of seven Rx or seven Tx 16-bit C-BUS registers which allow up to 104 bits (13 bytes) of data to be transferred at once. Raw or formatted data may be transmitted with the CMX7143 adding preamble, frame sync and tail bits.

Raw or formatted transmission/reception is selected using the Modem Mode and Control - $C1 write register, each whole transmission/reception must continue in the selected mode. Relevant registers are:

- Modem Mode and Control - $C1 write
- RxControl - $C3 write
- TxData0 - $B5 write (Plus TxData1-6)
- RxData0 - $B8 read (Plus RxData1-6)

Table 2 C-BUS Data Registers

C-BUS Address	Function	C-BUS address	Function
$B5	Tx data 0-7 & control	$B8	Rx data 0-7 & control
$B6	Tx data 8-23	$B9	Rx data 8-23
$B7	Tx data 24-39	$BA	Rx data 24-39
$CA	Tx data 40-55	$BB	Rx data 40-55
$CB	Tx data 56-71	$C5	Rx data 56-71
$C2	Tx data 72-87	$C9	Rx data 72-87
$C7	Tx data 88-103	$CC	Rx data 88-103
		$C3	RxControl

TxData0, RxData0 and RxControl hold a Transaction Counter. This a two-bit counter that is incremented on every read/write of the Data Block. This is particularly useful to detect data underflow and overflow conditions. The counter increments modulo 4.

The host must increment this counter on every write to the TxData block. If the CMX7143 identifies that a block has been written out of sequence, the Event IRQ will be asserted. The device detects that new data from the host is available by the change in the value of the Transaction Counter, therefore the host should ensure that all the data is available in the TxData block before updating this register (ie, it should be the last register the host writes to in any block transfer).

In Rx mode, the CMX7143 will automatically increment the counter every time it writes to the RxData block. If the host identifies that a block has been written out of sequence, then it is likely that a data overflow condition has occurred and some data has been lost. Two methods of data transfer are possible in receive mode, selectable using the UseTrans bit in the RxControl - $C3 write register.

If UseTrans is zero, the RxControl register bytewise flag and bit/byte counter is latched in at the start of the burst. Transfers containing eight or more bits must be selected as the CMX7143 will force a time delay between transactions to ensure that the host has sufficient time to read the RxData registers. Any writes to the transaction counter in the RxControl register will be ignored. Received data will be presented regularly in the RxData registers, with incrementing transaction count in RxData0 as it is received. Each transfer will contain the amount of data specified in the RxControl register at the start of the the burst. If UseTrans is zero then the RxControl register should not be written to during active reception.

If UseTrans is one, the transaction counter in the RxControl register controls the transaction size and rate during the burst. The CMX7143 will only output the next transaction when it sees that the transaction counter in the RxControl register has been incremented. When it is incremented the bit/byte count is read and the requested amount of data will be output in the RxData registers once available.

7.4.12 Raw Data Transfer

When transferring raw data the lowest 8 bits of the TxData0, RxData0 and RxControl registers are reserved for a Byte/Bit selector, Byte/Bit Counter and a Transaction Counter to allow the host to identify any data loss, and the remaining 104 bits hold the data to be transmitted/received. The byte count indicates how many bytes in the data block are valid and so reduces the need to perform a full, 7-word C-BUS read/write if only small blocks of data need to be transferred. The Byte/Bit selector provides a bit transfer mode which, while less efficient (in terms of C-BUS accesses to transfer a quantity of data), provides a facility to transmit or receive a burst of arbitrary length, not just a whole number of bytes. It is suggested that data is transferred in the maximum size blocks possible until the end of a burst - where the remaining bits, or bytes can be transferred in a single transaction of the required size.

7.4.13 Formatted Data Transfer

When the transfer of formatted data is selected by the Modem Mode and Control - $C1 write register the TxData0, RxData0 and RxControl registers indicate the block type to use in either sending or decoding the data. The block type dictates the format or quantity of data transferred.

7.4.14 Pre-loading Transmit Data

It is possible to pre-load a number of transactions into the CMX7143 before transmission begins. To do this the host should load the first transaction into the TxData registers and then select Transmit (Idle) or Carrier Sense (Idle) mode. The first transaction will be loaded into the CMX7143 but no transmission will begin. Further transactions may be loaded in, creating a larger buffer of data than the TxData registers can hold themselves. Once the buffer is full the CMX7143 will stop accepting transactions. Next, an active Tx mode should be selected by the host and the data in the buffer will be transmitted, allowing the host to load further transactions as the buffer becomes free.

The buffer of pre-loaded data may be created in Carrier Sense (Idle) and Transmit (Idle) modes simply because in those modes no data is being transmitted - so the buffer does not empty. Transactions and buffering are carried out in an otherwise identical fashion in the active Transmit or Carrier Sense modes. When using the Modem Control bits in $C1 to change from an active Transmit or Carrier Sense mode into Transmit (Idle) or Carrier Sense (Idle) mode, or back again into an active mode, sufficient time must be allowed for the change of mode to be recognised by the CMX7143. As there is no flag to indicate when the previous mode change has been actioned, a delay of 3 x AuxClk periods should be inserted between a mode change and further C-BUS writes.

The buffer is cleared when the host changes the lower two bits of the modem control register or following an automatic transition from Carrier Sense mode into Receive mode.

7.4.15 Auxiliary Clock Rates

Auxiliary functions including carrier sensing, AuxADC, DAC and GPIO updates operate on an internal clock. This rate will be referred to in describing these functions. The AuxClk speed is given by:

In Idle: AuxClk = Xtal Frequency / (P3.2 x (P3.3 – 128) x 8)

In Tx: if P3.7 less than 256: AuxClk = symbol rate x 5/2
In Tx: if P3.7 more than 256: AuxClk = symbol rate x 5

In Rx/CS: AuxClk = symbol rate x 5/2

7.4.16 Auxiliary Data

The CMX7143 provides 2 auxiliary data registers. These can each be independently configured to output the following information:

- AuxADC1 input data and threshold detect status
- AuxADC2 input data and threshold detect status
- The input on 4 x GPIO pins if configured as inputs
- The dc offset of any signal in the process of being received, based on the selected RxSig input
- The RSSI of any signal, based on the selected RSSI input

The information is selected using the AuxConfig register. See:

- AuxConfig - $A7 write
- Aux Data1 - $A9 read
- Aux Data2 - $AA read

7.4.17 GPIO Pin Operation

The CMX7143 provides 4 x GPIO pins, each pin can be configured independently as automatic/manual, input/output and rising/falling (with the exception of the combination automatic + input which is only allowed for GPIO1).

Pins that are automatic outputs become part of a transmit sequence and will automatically switch, along with the RAMDAC (if it is configured as automatic) during the course of a burst. Pins that are manual are under direct user control. When automatic, a rising or a falling event at the start or end of transmission will cause the specified GPIO to get switched high or low accordingly.

GPIO1 may be configured as an automatic input. This means that any attempted transmission will wait until GPIO1 input is high (if rising is selected) or low (if falling is selected).

See:

- Program Block 1 – Burst Tx Sequence + GPIO Configuration
- AuxConfig - $A7 write
- Aux Data1 - $A9 read
- Aux Data2 - $AA read
- AuxConfig2 - $CD write

7.4.18 Auxiliary ADC Operation

The inputs to the two Auxiliary ADCs can be independently routed to any of the Signal Input pins under control of the Signal Routing register $A7. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to “off”. BIAS in the Power Down Control - $C0 write register must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the Signal Routing register $A7, the length of the averaging is determined by the value in the Program Block (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in P3.0 and P3.1. For an average value of 0; 50% of the current value will be applied, for a value of 1 = 25%, 2 = 12.5% etc. The maximum useful value of this field is 8.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated as required (except in the case where the high threshold has been set below the low threshold). The thresholds are programmed via the AuxADC Threshold register $CD.

Auxiliary ADC data is read back in the AuxADC Data registers $A9 and $AA and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

The AuxADC sample rate is affected by settings in Program Block 3 – RAMDAC and Clock Control. The rate will be the AuxClk rate, see 7.4.15 Auxiliary Clock Rates.

See:

- AuxConfig - $A7 write
- Aux Data1 - $A9 read
- Aux Data2 - $AA read
- AuxConfig2 - $CD write

7.4.19 Auxiliary DAC/RAMDAC Operation

The four Auxiliary DAC channels are programmed via the AuxDAC Control register $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will autonomously output a pre-programmed profile at a programmed rate. The RAMDAC may be configured as automatic or manual using Program Block 1 – Burst Tx Sequence + GPIO Configuration. The AuxDAC Control register $A8, with b12 set, controls the RAMDAC mode of operation when configured as a manually triggered RAMDAC.

The default profile is a raised cosine (see Table 6 in the User Manual), but this may be over-written with a user defined profile by writing to Program Block 3. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Control register $A8 and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

See:

- AuxDAC Control/Data - $A8 write

7.5 Digital System Clock Generators

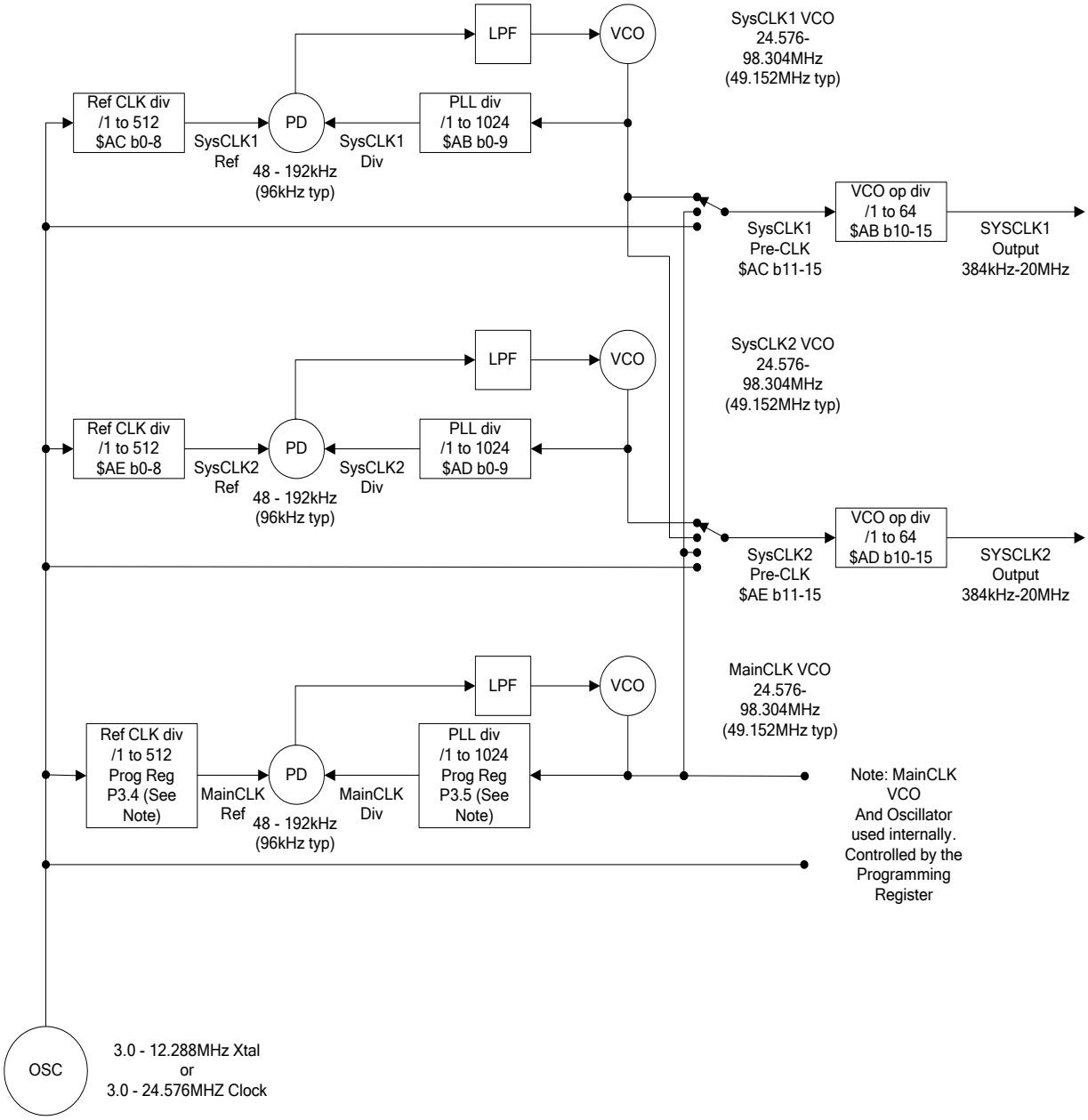


Figure 12 Digital Clock Generation Schemes

The CMX7143 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 5, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency is expected to be 9.6MHz, if an external oscillator is used the input frequency can be 9.6 or 19.2MHz.

7.5.1 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 12. Note that the output is inhibited until enabled by a host command over the C-BUS. See:

- System Clk 1 and 2 PLL data - $AB, $AD write
- System Clk 1 and 2 REF - $AC and $AE write

7.5.2 Main Clock Operation

A digital PLL is used to create the Main Clock for the internal sections of the CMX7143. The configuration of the main clock and the internal clocks derived from it is controlled using Program Block 3 – RAMDAC and Clock Control.

The CMX7143 defaults to settings appropriate for a 19.2MHz Xtal with a baud rate of 9600s/s, however if a 9.6MHz crystal is to be used, or a different baud rate required then Program Block entries P3.2 to P3.6 will need to be programmed appropriately at power-on. A table of allowed values is provided in Table 5.

It is possible to route the output from the Main clock VCO to the VCO output dividers for either SYSCLK1 or SYSCLK2 output frequency generation. However, as the Main clock VCO output is used internally there are constraints on selection of its frequency. The frequency will be based on Program Block P3.4 and P3.5, with allowed values given in Table 5 Xtal/Clock Frequency Settings for Program Block 3. Additionally, as the CMX7143 disables the Main clock VCO during Idle mode, this selection will only be of use during the active modes of the device.

See:

- Program Block 3 – RAMDAC and Clock Control
- System Clk 1 and 2 REF - $AC and $AE write
- Table 5 Xtal/Clock Frequency Settings for Program Block 3

7.6 Signal Level Optimisation

The internal signal processing of the CMX7143 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts p-p = 838mV rms, assuming a sine wave signal. This should not be exceeded at any stage.

7.6.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The Fine Output adjustment has a maximum attenuation of 1.8dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 44.8dB and no gain.

7.6.2 Receive Path Levels

The Fine Input adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input adjustment has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the CH1FB, CH2FB or CH3FB pin would be 838mV rms.

7.7 C-BUS Register Summary

Table 3 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxConfig	16
$A8	W	AuxDAC Control/Data	16
$A9	R	Aux Data1/Checksum 2 hi	16
$AA	R	Aux Data2/Checksum 2 lo	16
$AB	W	System Clk 1 PLL data	16
$AC	W	System Clk 1 Ref	16
$AD	W	System Clk 2 PLL data	16
$AE	W	System Clk 2 Ref	16
$AF		Reserved	
$B0		Reserved	
$B1	W	Input Gain and Input/Output Signal Routing	16
$B2		Reserved	
$B3		Reserved	
$B4		Reserved	
$B5	W	TxData0	16
$B6	W	TxData1	16
$B7	W	TxData2	16
$B8	R	RxData0/Checksum 1 hi	16
$B9	R	RxData1/Checksum 1 lo	16
$BA	R	RxData2	16
$BB	R	RxData3	16
$BC		Reserved	
$BD		Reserved	
$BE		Reserved	
$BF		Reserved	
$C0	W	Power-Down Control	16
$C1	W	Modem Mode and Control	16
$C2	W	Tx Data5	16
$C3	W	Rx Control	16
$C4		Reserved	
$C5	R	Rx Data4	16
$C6	R	Status	16
$C7	W	TxData6	16
$C8	W	Programming Register	16
$C9	R	RxData5	16
$CA	W	TxData3	16
$CB	W	TxData4	16
$CC	R	RxData6	16
$CD	W	AuxConfig2	16
$CE	W	Interrupt Mask	16
$CF		Reserved	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8 7143FI-2.x Features

The 7143FI-2.x uses a 4FSK modulation scheme with a configurable over-air bit rate up to 20,000bps (ie: 10,000 symbols per second). Raw data can be transferred, in addition to formatted data blocks. Formatted data blocks may be of variable length – up to 12 bytes and support a combination of 16-bit or 32-bit CRC for error detection, plus trellis coding for error correction. The modulation scheme and coding is designed to produce a signal that is over-the-air compatible with the CML FX/MX919B and CMX969 (RD-LAP) modems.

8.1 Modulation

The 4FSK scheme running at 2400 symbols/s (4800 bits/s) can be used to fit inside a 6.25kHz channel bandwidth, a rate of 9600 symbols/s can be used in 25kHz bandwidth channels. A 12.5kHz channel bandwidth is possible with data rates in between these extremes. Channel bandwidth is dependent on the peak deviation that the modulating signal causes the carrier to deviate by as well as the data rate.

Note: In I/Q output mode when operating above 5,000 symb/s users should be aware that excessive deviation will cause degradation of the modulation. For some typical results see Figure 24, section 8.5. Note that these results illustrate operation with a deviation that is not excessive, therefore no degradation is present.

The bit to symbol mapping that this Function Image™ uses is:

Input Bit Pair	Relative Symbol Level
00	-1
01	-3
10	+1
11	+3

RRC filters are implemented at both Tx and Rx with a filter alpha of 0.2.

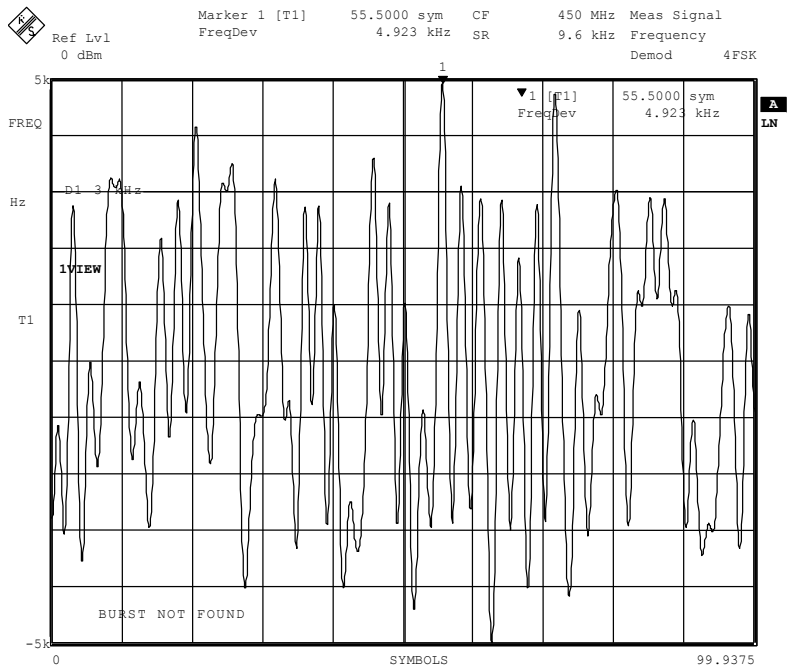


Figure 13 4FSK PRBS Waveform

8.2 Radio Interface

The CMX7143 is designed to process a demodulated signal from a limiter/discriminator source, therefore for optimum performance, it is important that the demodulated signal is not significantly degraded by narrow filters and/or group delay distortion. The CMX7143 can be configured to output a 2-point modulation signal, or a modulated I/Q output signal with programmable deviation. An overview of how the CMX7143 might integrate with a limiter discriminator receiver and 2-point modulation transmitter is shown in Figure 14.

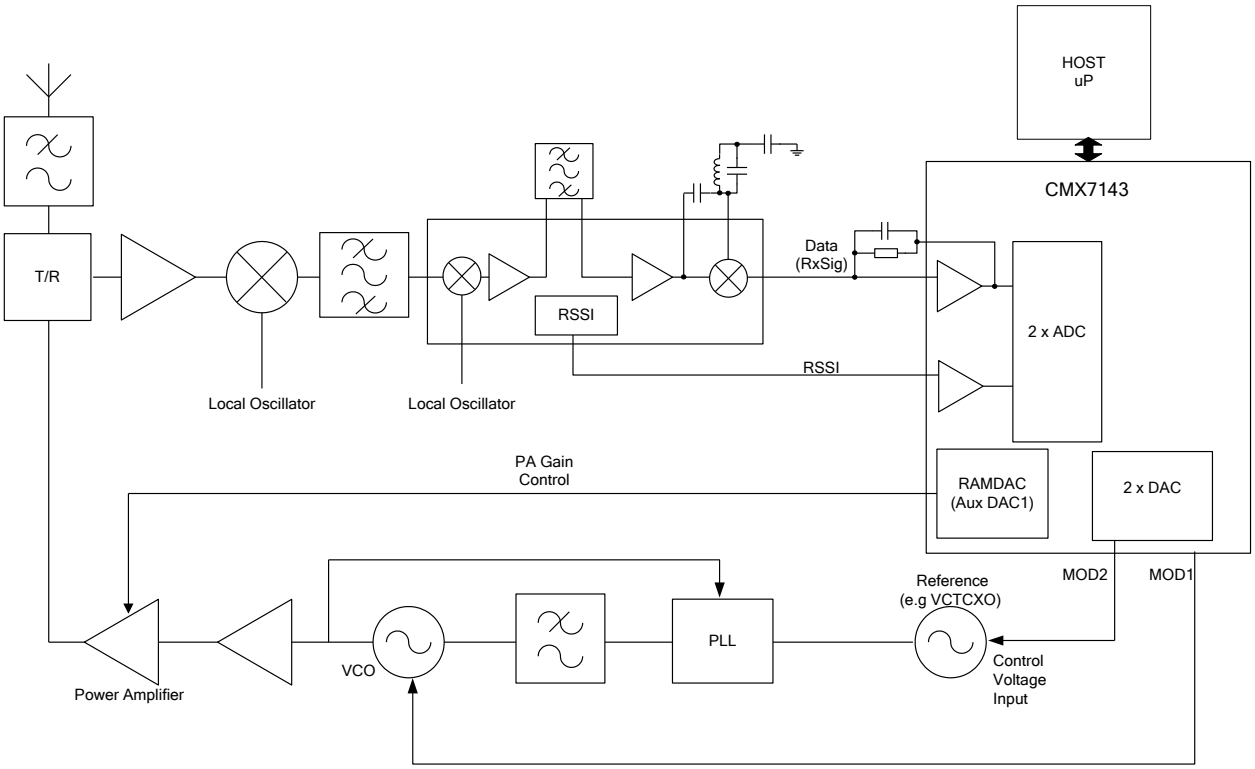


Figure 14 Outline Radio Design

8.3 Formatted Data

The 7143FI-2.x supports two kinds of formatted data – native formatted data and RD-LAP formatted data, both of which provide the ability to channel code blocks of data using trellis coding and CRCs.

Native Formatted Data:

The frame structure as used in a formatted data system is illustrated in Figure 15. It typically consists of a 24-symbol frame sync pattern followed by a 'Header Block', one or more 'Intermediate Blocks and a 'Last Block'.

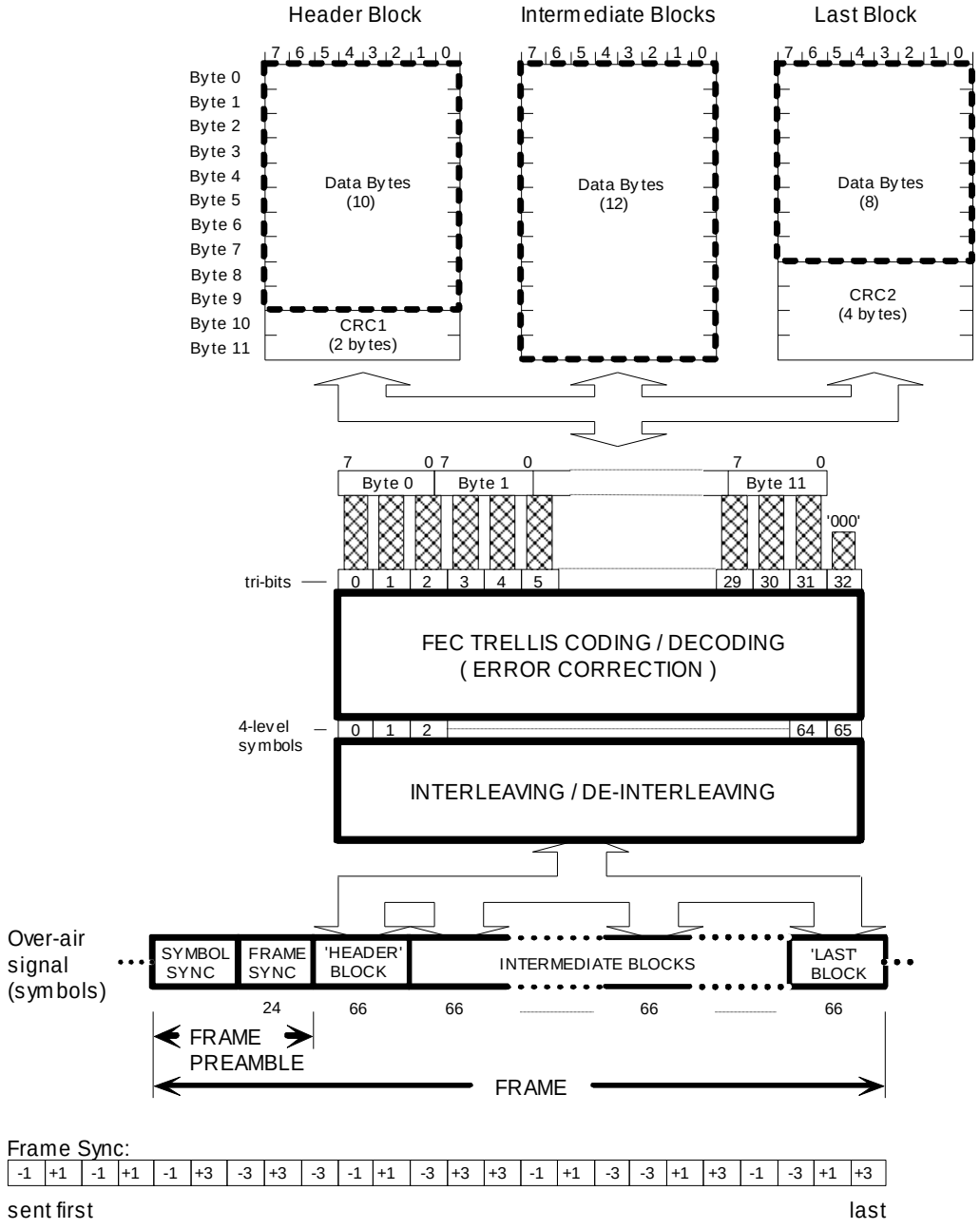


Figure 15 Formatted Data Over Air Signal Format

The 'Header' block is self-contained in that it includes its own checksum (CRC1), and would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any) and miscellaneous control information.

The 'Intermediate' block(s) contain only data; the checksum at the end of the 'Last' block (CRC2) also checks the data in any preceding 'Intermediate' blocks. This checksum calculation should be reset as required using the “Reset CRC2” block type – so that any transmitted CRC2 contains the CRC of only the desired blocks. In receive it must be reset to match the expected input data block sequence. For example: To CRC only the data in the intermediate blocks + one last block pictured in Figure 15, a “reset CRC2” block should be sent before the first intermediate block – with the same sequence duplicated in receive.

Proprietary systems which do not use the standard formatted data block structures may use the block structures provided by the CMX7143 to build alternative frame formats more suited to the particular application. Some examples are illustrated in Figure 16.

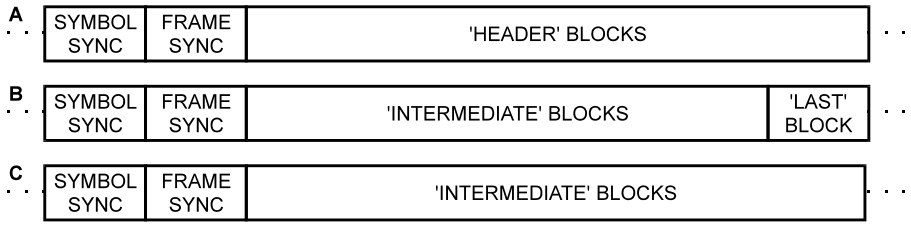


Figure 16 Some Alternative Frame Structures

The CMX7143 performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC being that enclosed by the thick dashed rectangles near the top of Figure 15. When receiving header blocks and last blocks, the CMX7143 will indicate CRC success or failure and will provide the data regardless.

In Figure 15 the size of data block illustrated is always 12 bytes when user bytes and CRC bytes are counted together. The CMX7143 adds further flexibility by supporting block sizes of 6 or 9 bytes total, the resulting data content being:

Block Type Specifier	user bytes	CRC bytes
12 byte header block	10	2
12 byte intermediate block	12	0
12 byte last block	8	4
6 byte header block	4	2
6 byte intermediate block	6	0
6 byte last block	2	4
9 byte header block	7	2
9 byte intermediate block	9	0
9 byte last block	5	4
Reset CRC2	N/A	N/A
Insert preamble	N/A	N/A
Insert FS1	N/A	N/A
Insert FS2	N/A	N/A

RD-LAP Formatted Data:
The frame structure in RD-LAP mode is illustrated in Figure 17 RD-LAP Over Air Signal Format, and typically consists of a Frame Preamble (comprising a 24-symbol Frame Synchronisation pattern and Station ID block) followed by one or more 'Header’ blocks, one or more 'Intermediate’ blocks and a 'Last’

block. Channel Status (S) symbols are included at regular intervals. The first frame of any transmission is preceded by a Symbol Synchronisation pattern.

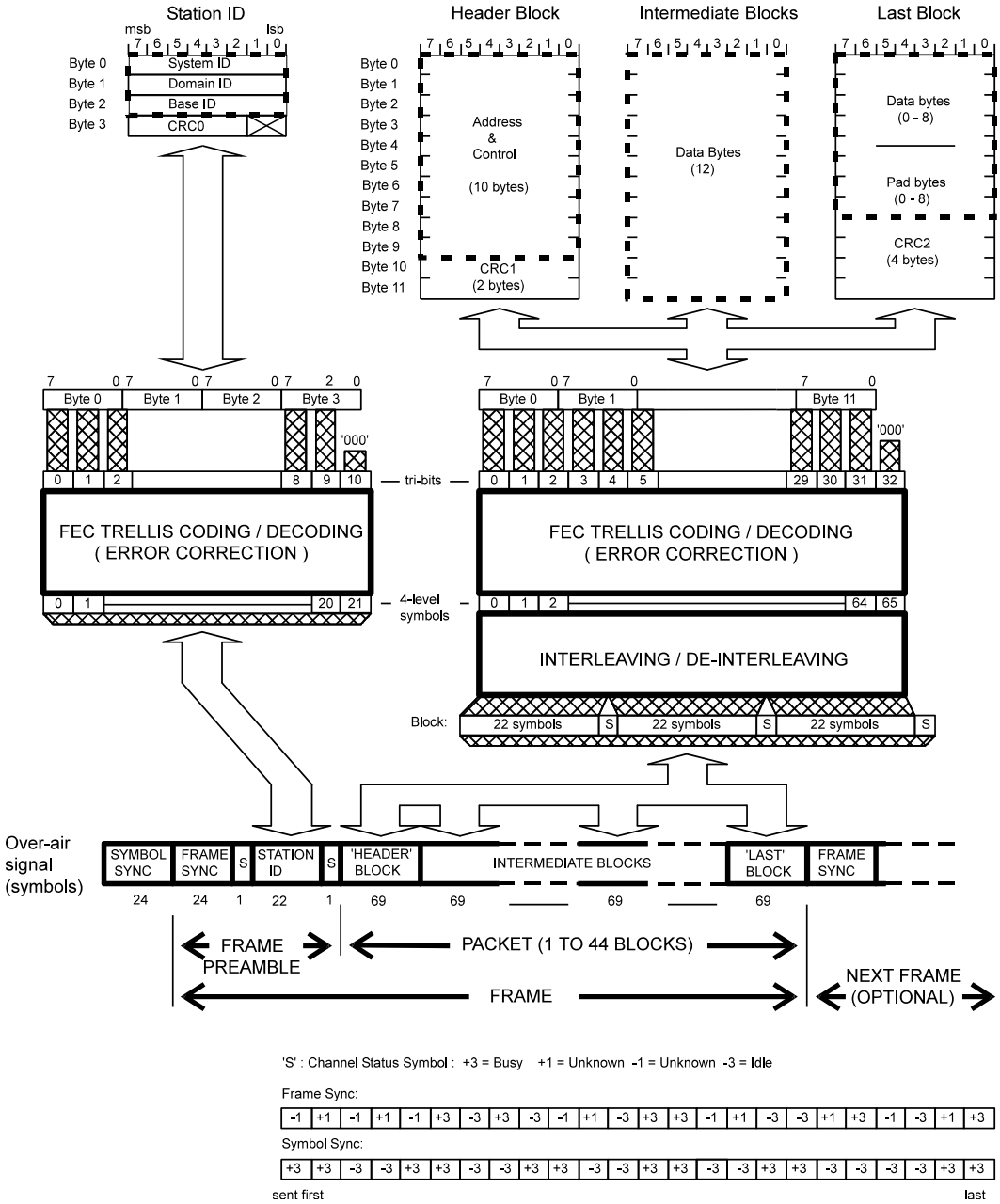


Figure 17 RD-LAP Over Air Signal Format

The ‘Station ID’ and the ‘Header’ block are self-contained as they include their own checksums – CRC0 (6-bit CRC) and CRC1 (16-bit CRC) respectively.

The 'Intermediate' block(s) contain only data. The checksum at the end of the 'Last' block (CRC2 – 32-bit CRC) also checks the data in any preceding 'Intermediate' blocks. This checksum calculation should be reset as required using the ‘Reset CRC2’ block type – so that any transmitted CRC2 contains the CRC of only the desired blocks. In receive it must be reset to match the expected input data block sequence.

The CMX7143 performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC being that enclosed by the thick dashed rectangles near the top of Figure 17. When receiving header blocks and last blocks, the CMX7143 will indicate CRC success or failure and will provide the data regardless.

In Figure 17 the size of data block illustrated is always 12 bytes when user bytes and CRC bytes are counted together. The channel status symbols must be packed in a byte and provided along with the payload data as shown in TxData0 - $B5 write (Plus TxData1-6) register.

Note that in order to be compatible with CMX969 RD-LAP coding the initial CRC value must be configured to 0 as shown in Program Block 0 – Burst Data Configuration.

8.4 Cyclic Redundancy Codes

CRC0
This is a six-bit CRC check code used in the Station ID Block. It is calculated by the modem from the first 24 bits of the block (Bytes 0,1 and 2) as follows:

The 24 bits are considered as the coefficients of a polynomial M(x) of degree 23, such that the msb bit (7) of byte 0 is the coefficient of x^{23}, and bit 0 of byte 2 is the coefficient of x^0.

The polynomial F(x) of degree 5 is calculated as being the remainder of the modulo-2 division

$$x^6M(x) / (x^6 + x^4 + x^3 + 1)$$

The polynomial $x^5 + x^4 + x^3 + x^2 + x^1 + x^0$ is added (modulo-2) to F(x)

The coefficients of F(x) are placed in the 6-bit CRC0 field, such that the coefficient of x^5 corresponds to the msb of CRC0.

CRC1
This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block. It is calculated by the modem from the first 80 bits of the block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

CRC2
This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$$

Notes:

The CRC2 checksum calculation should be reset as required using the “Reset CRC2” block type specifier (see Figure 16) – so that any transmitted CRC2 contains the CRC of only the desired blocks. In receive, CRC2 must be reset to match the expected input data block sequence.

Program Block P0.10 allows the user to select between two different forms of the CRC0, CRC1 and CRC2 checksums, by changing the initial value of the CRC generator. See section 10.2.2. By default P0.10 is set to all ‘1’s (suitable for CCITT X25 based systems). Setting P0.10 to all ‘0’s is required for RD-LAP (CMX969) compatibility.

8.5 Transmit Performance

The Tx modulation may be evaluated using a suitable signal generator, modulated by the CMX7143, the output of which may be measured on a spectrum/modulation analyser (see Figure 18).

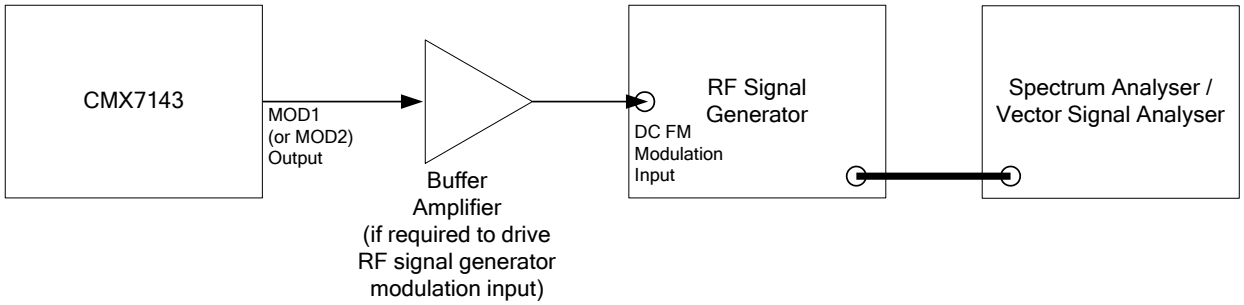
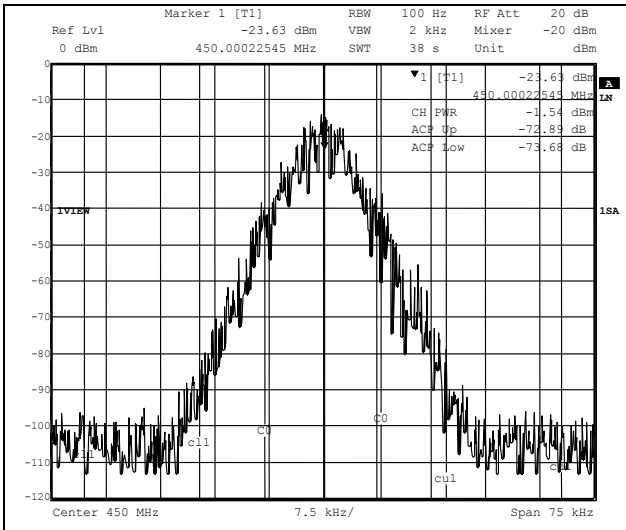


Figure 18 Tx Spectrum and Modulation Measurement Configuration

Using the test system of Figure 18 some typical results are shown in the following figures. The internal PRBS generator was used to generate the data in all the results shown. The desired deviation was achieved by adjusting the CMX7143 output level and/or the peak deviation programmed on the RF Signal Generator.

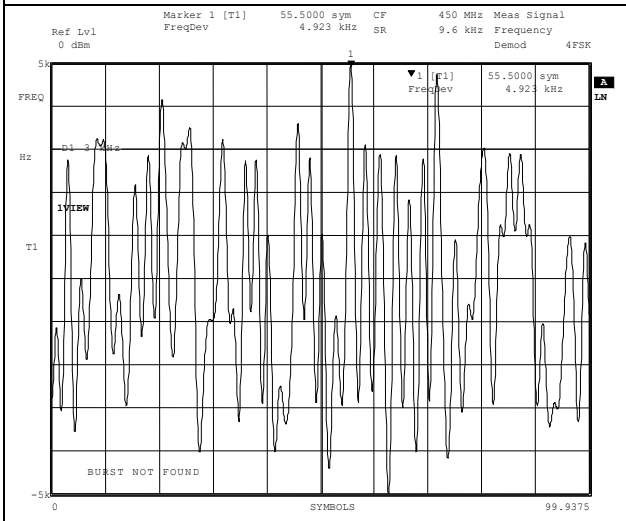


Modulation spectrum (left)

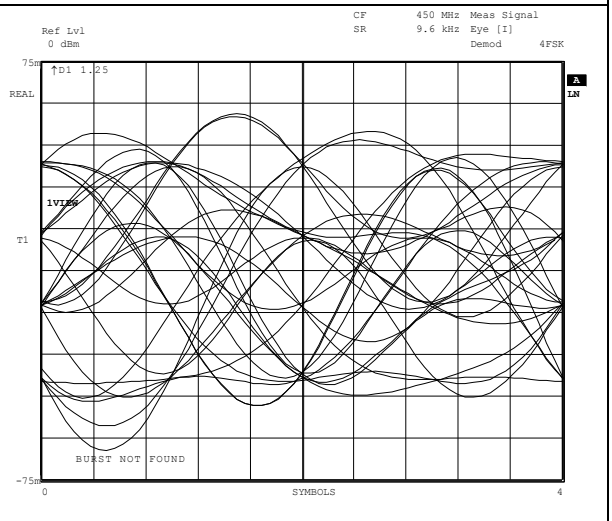
EN 300 113 Adjacent Channel measurement for 25kHz channel:

ACP = -73dB

(RBW=100Hz, Integration window = 16kHz)

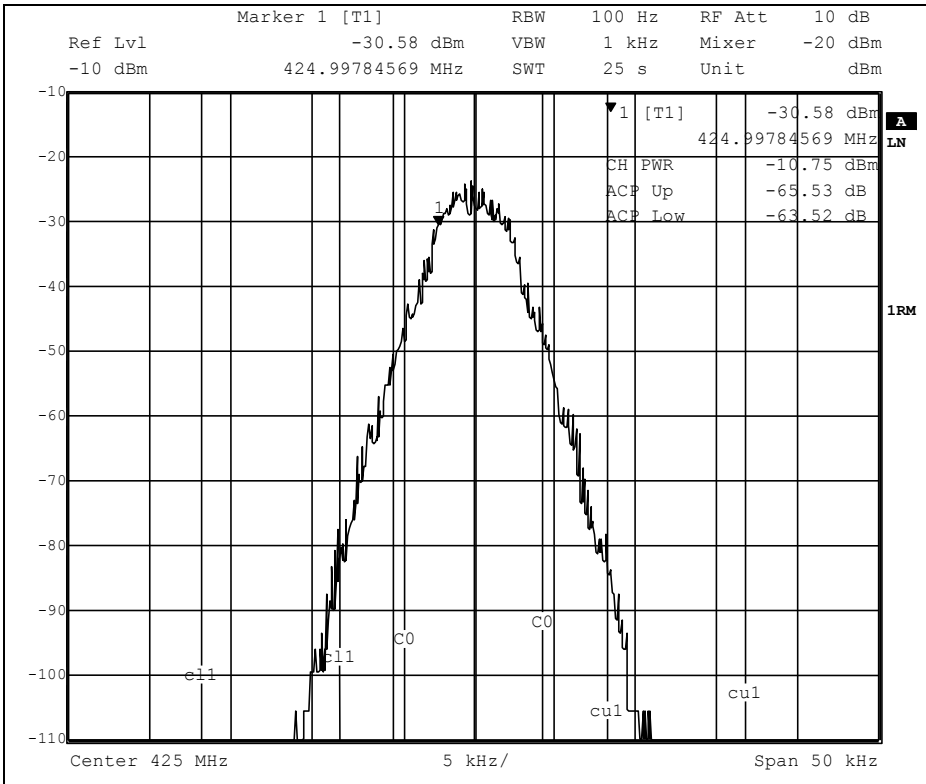


Deviation (<5kHz, Deviation for +3 symbol = 3kHz)



Eye Diagram

Figure 19 Tx Modulation Spectra (4FSK), 19200bps, 2-point modulation

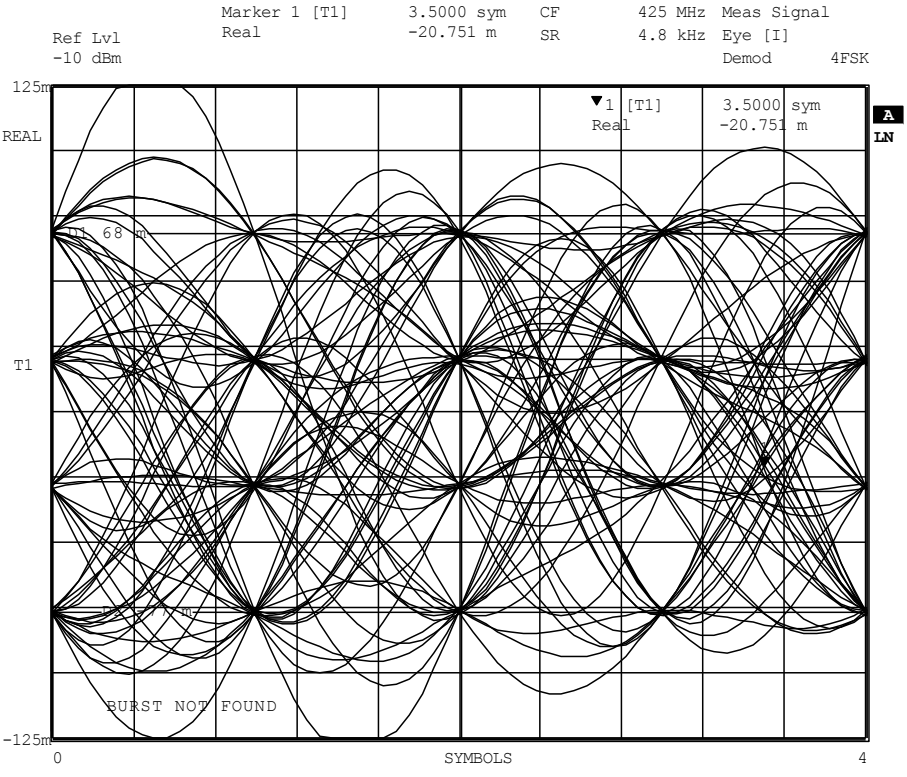


Modulation spectrum

EN 300 113 Adjacent Channel measurement for 12.5kHz channel:

ACP < -63dB (limit is –60dB)

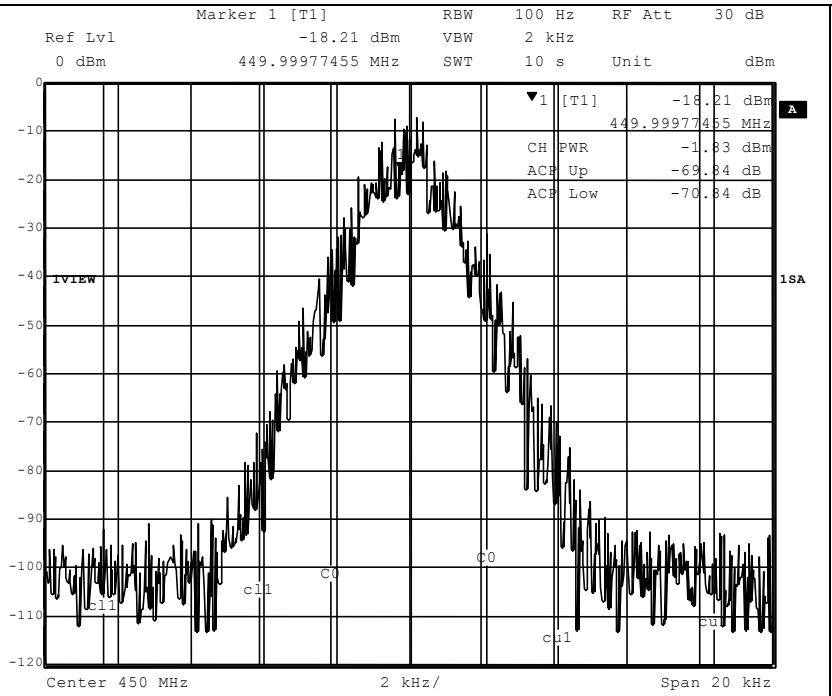
(RBW=100Hz, Integration window = 8.5kHz, detector =r.m.s.)



Eye Diagram

Deviation for +3 symbol = 1.75 kHz)

Figure 20 Tx Modulation Spectra (4FSK), 9600bps (4800 symb/s), 2point modulation



Modulation spectrum

EN 301 166 for 6.25kHz channels. Deviation +/-1kHz for +3 symbol.

Adjacent channel power = -70dB (limit is –60dB)

RBW=100Hz, Integration bandwidth = 70% of the channel spacing

Figure 21 Tx Modulation Spectra (4FSK), 4800bps – 2-point modulation

The CMX7143 also generates modulation in I/Q format. A test system is shown in Figure 22 and results in Figure 23 and Figure 24. As will be observed the spectrum meets the requirements of EN 300 113.

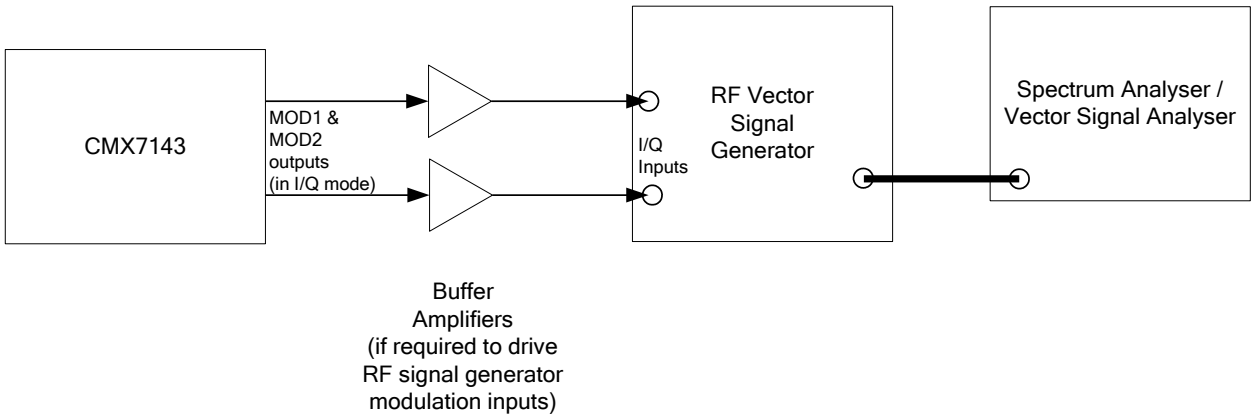
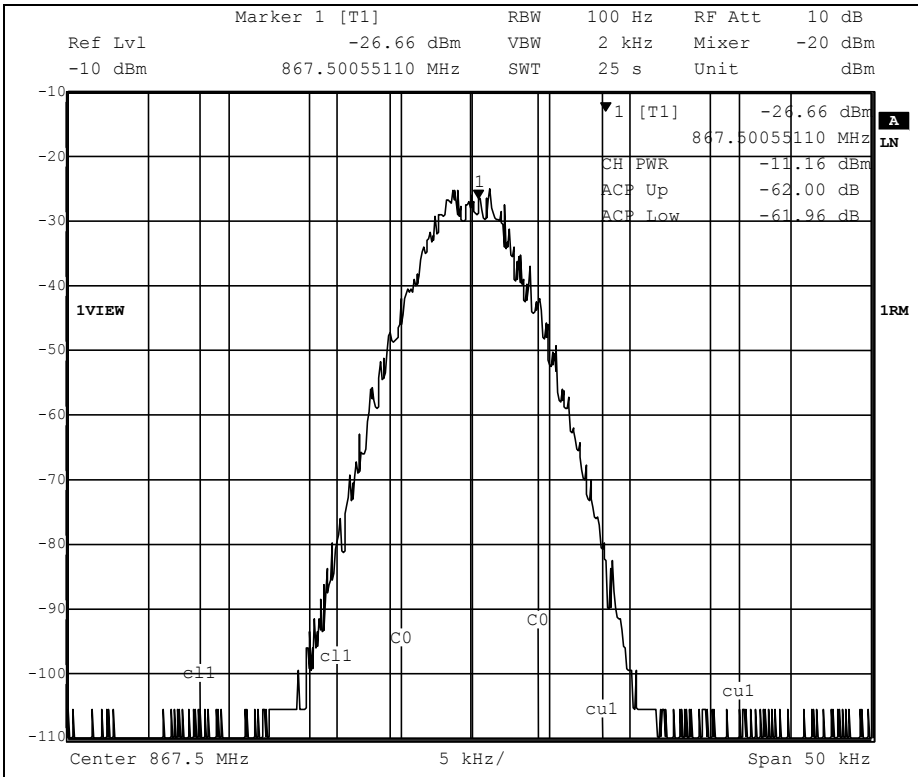


Figure 22 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation

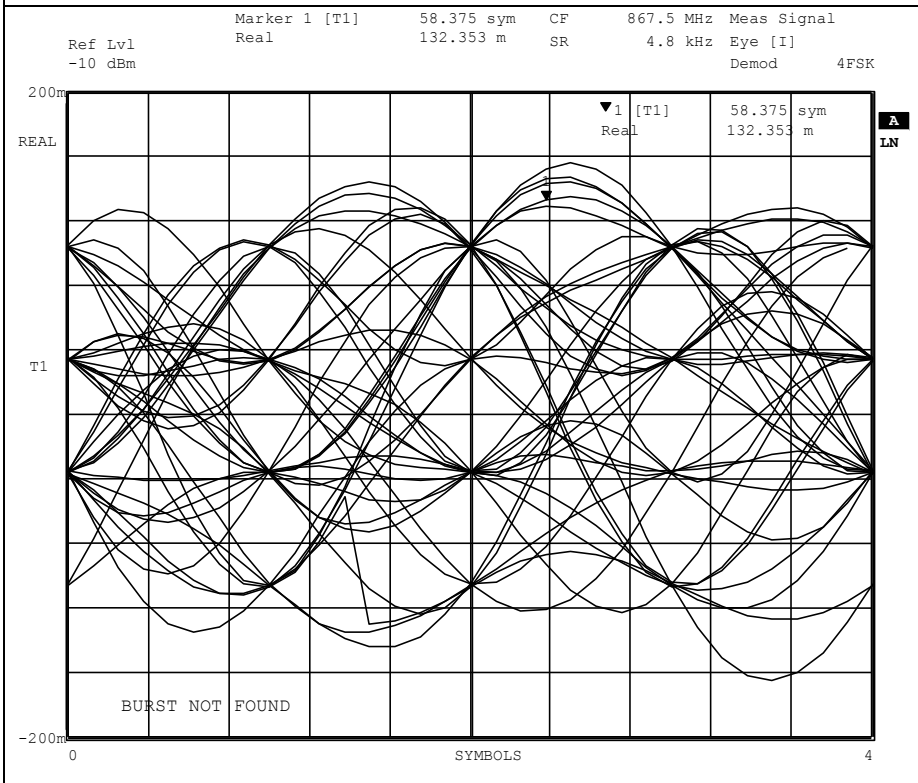


Modulation spectrum

EN 300 113 Adjacent Channel measurement for 12.5kHz channel:

ACP < -62dB (limit is –60dB)

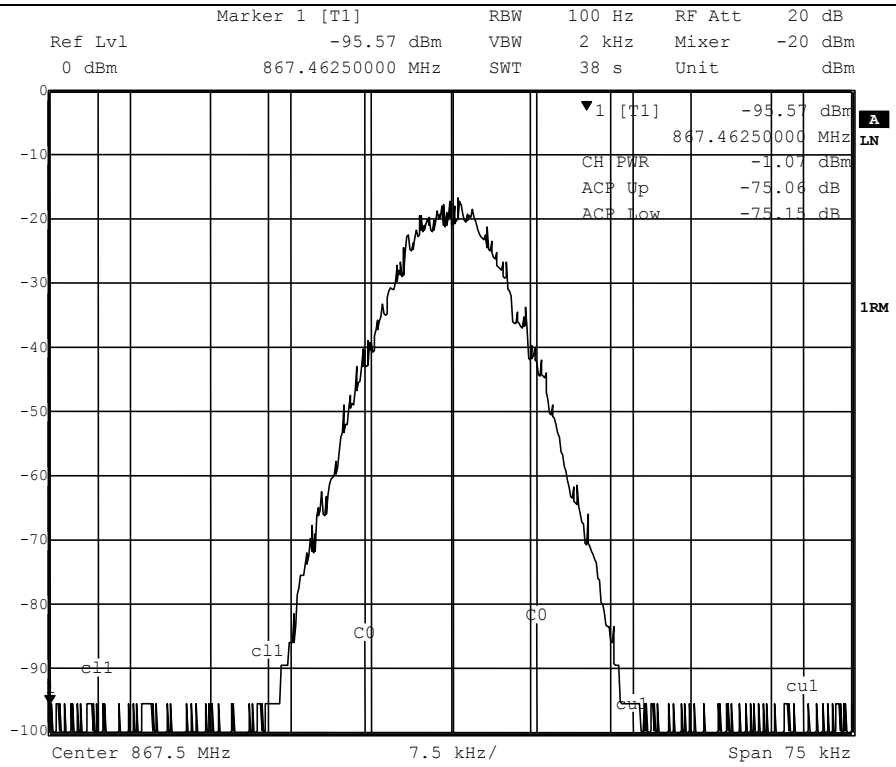
(RBW=100Hz, Integration window = 8.5kHz, detector =r.m.s.)



Eye Diagram

Deviation for +3 symbol = 2.05 kHz)

Figure 23 Tx Modulation Spectra (4FSK), 9600bps (4800 symb/s), I/Q modulation

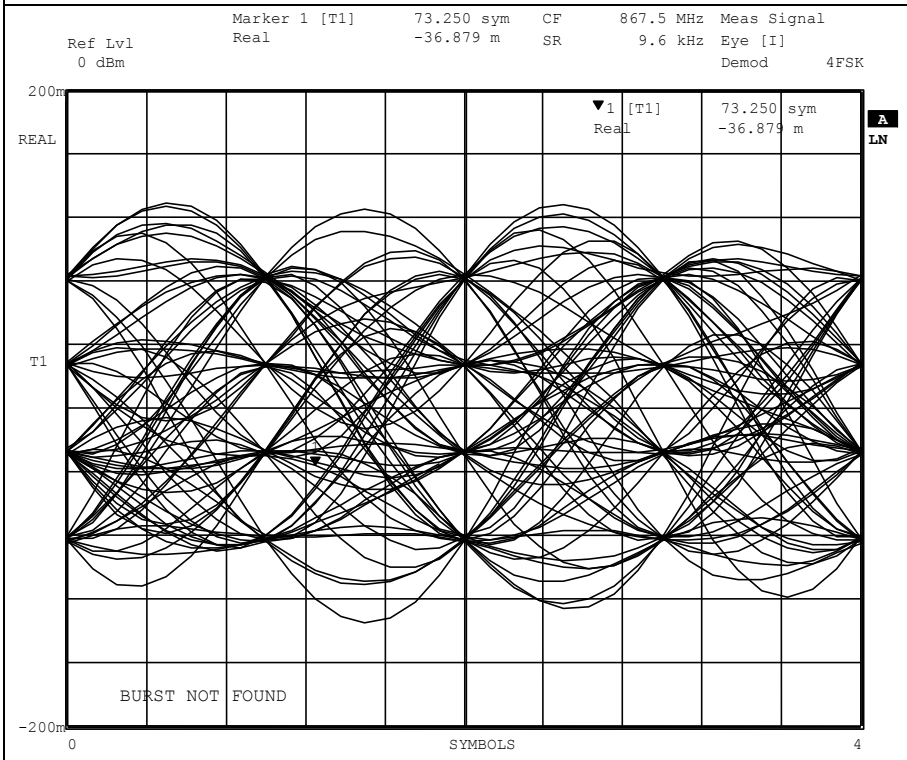


Modulation spectrum

EN 300 113 Adjacent Channel measurement for 25kHz channel:

ACP < -75dB (limit is –70dB)

(RBW=100Hz, Integration window = 16kHz, detector =r.m.s.)



Eye Diagram

Deviation for +3 symbol = 3.2 kHz)

Figure 24 Tx Modulation Spectra (4FSK), 19200bps (9600 symb/s), I/Q modulation

8.6 Receive Performance

The performance of the receiver will be different for any combination of bit-rate and deviation. To aid the designer, some typical performance data has been measured using a realistic FM receiver. Results using the CMX7143 connected to the receiver demodulated signal output are available as a CML Application Note in the Design Support – Wireless Data section of the CML website [www.cmlmicro.com].

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD} - DV_{SS}	–0.3	4.5	V
AV_{DD} - AV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD} or DV_{SS})	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using a Xtal)	11	9.6	9.6	MHz
XTAL/CLK Frequency (using an external clock)	11	9.6	19.2	MHz

Notes: 11 Nominal XTAL/CLK frequency is 9.6MHz or 19.2MHz

12 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.

9.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz±0.01% (100ppm); T_{AMB} = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
V_{DEC} = 2.5V
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device when loaded with FI-2.x only. The use of other Function Images™, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	22				
DI_{DD}		–	2.1	–	mA
AI_{DD}		–	4	–	µA
Rx Mode	22				
DI_{DD} (4800bps – search for FS)		–	6.6	–	mA
DI_{DD} (9600bps – search for FS)		–	10.8	–	mA
DI_{DD} (19200bps – search for FS)		–	19.2	–	mA
DI_{DD} (4800bps – FS found)		–	4.1	–	mA
DI_{DD} (9600bps – FS found)		–	5.6	–	mA
DI_{DD} (19200bps – FS found)		–	8.7	–	mA
AI_{DD}		–	3.2	–	mA
Tx Mode	22				
DI_{DD} (4800bps – 2-point)		–	10.2	–	mA
DI_{DD} (9600bps – 2-point)		–	12.7	–	mA
DI_{DD} (19200bps – 2-point)		–	12.7	–	mA
DI_{DD} (4800bps – I/Q)		–	11.3	–	mA
DI_{DD} (9600bps – I/Q)		–	14.4	–	mA
DI_{DD} (19200bps – I/Q)		–	14.7	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	3.1	–	mA
Additional current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes: 21 T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
22 System Clocks, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	25				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input current (Vin = DV_{DD})		–	–	40	µA
Input current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	21	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 120µA)		90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current	21	–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
RDATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output voltage offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output impedance		–	22	–	kΩ

Notes: 25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' pulse width		31	15	–	–	ns
'Low' pulse width		31	15	–	–	ns
Input impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal start up (from powersave)			–	20	–	ms
SYSCLK1/2 Outputs						
XTAL/CLK input to SYSCLK1/2 timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' pulse width		33	48	52.08	56	ns
'Low' pulse width		33	48	52.08	56	ns
V_{BIAS}						
Start up time (from powersave)			–	30	–	ms
CH1, 2 and 3 Inputs (RxSig/RSSI 1, 2 and 3)						
Input Impedance		34	–	1	–	MΩ
Maximum Input Level (p-p)		35	–	–	80%	AV_{DD}
Load resistance (feedback pins)			80	–	–	kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)			–	80	–	dB
Unity gain bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 9.6MHz XTAL fitted and 9.6MHz output selected.

34 With no external components connected

35 Centered about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: CH1FB, CH2FB or CH3FB.

37 Design value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 (MOD1, MOD2)					
Power-up to output stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output current range (AV_{DD} = 3.3V)		–	–	±125	µA
Output voltage range	44	0.5	–	AV_{DD} –0.5	V
Load resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centered about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (ADC1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10-bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (p-p)	54	–	–	80%	AV_{DD}
Conversion time	52	–	59.9	–	µs
Input impedance					
Resistance		–	10	–	MΩ
Capacitance		–	5	–	pF
Zero error (input offset to give ADC output = 0)		0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10-bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (p-p), no load	54	80%	–	–	AV_{DD}
Zero error (output offset from a DAC input = 0)		0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

9.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz ±0.01% (100ppm); T_{AMB} = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
V_{DEC} = 2.5V
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.
All figures quoted in this section apply to the device when loaded with F-I2.x only. The use of other Function Images™ can modify the parametric performance of the device.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Modem symbol rate		2000		10000	sym s^{-1}
Modulation			4FSK		
Filter RRC alpha			0.2		
Tx bit rate accuracy	63		-		ppm
Tx output level (MOD1, MOD2, 2-point)	64		2.1		Vp-p
Tx output level (MOD1, MOD2, I/Q)	64		2.1		Vp-p
Tx adjacent channel power (MOD1, MOD2, PRBS)	65		-73		dB
Rx co-channel rejection	67		12		dB
Rx input level	66			838	mVrms
Rx input dc offset	66		1.6		V

Notes:

63	Determined by the accuracy of the Xtal oscillator provided
64	Transmitting continuous default preamble
65	Measured as per EN 301 166 or EN300 113 as appropriate. See section 8.5.
66	The combined effect of Rx input level and the Rx input dc offset must be such that the wanted signal envelope always lies within 10% to 90% of AV_{DD}.
67	Typical for 1% BER but depends on deviation and other radio parameters. For more information see application note available from www.cmlmicro.com.

9.2 C-BUS Timing

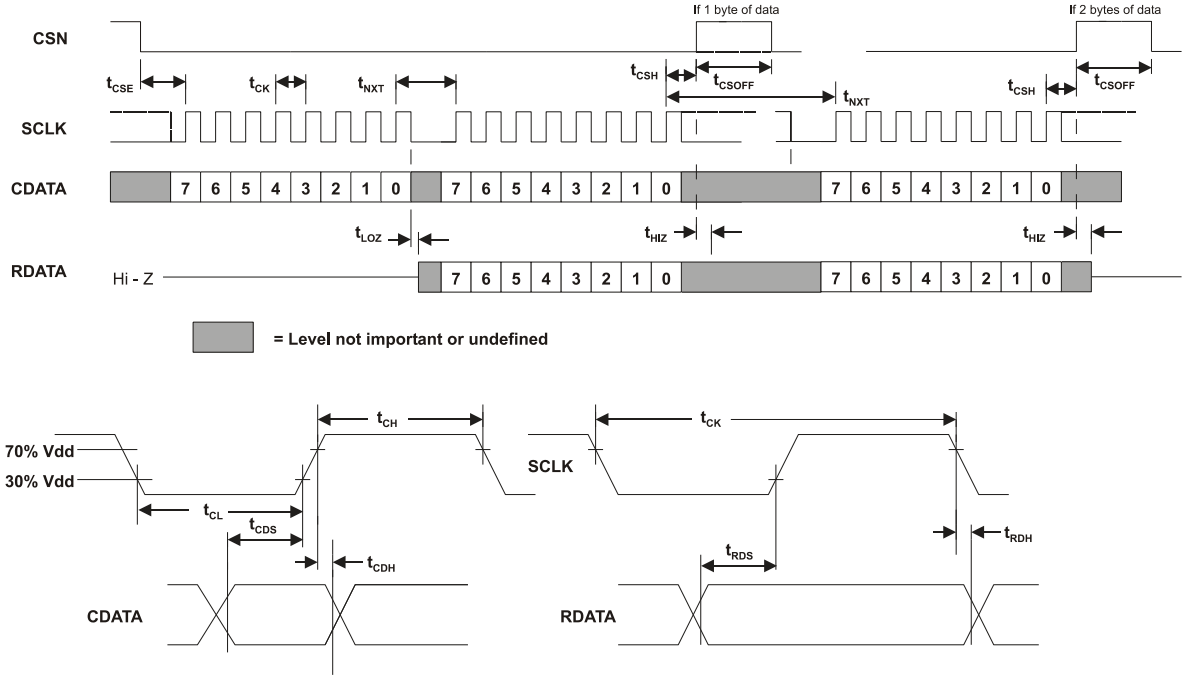


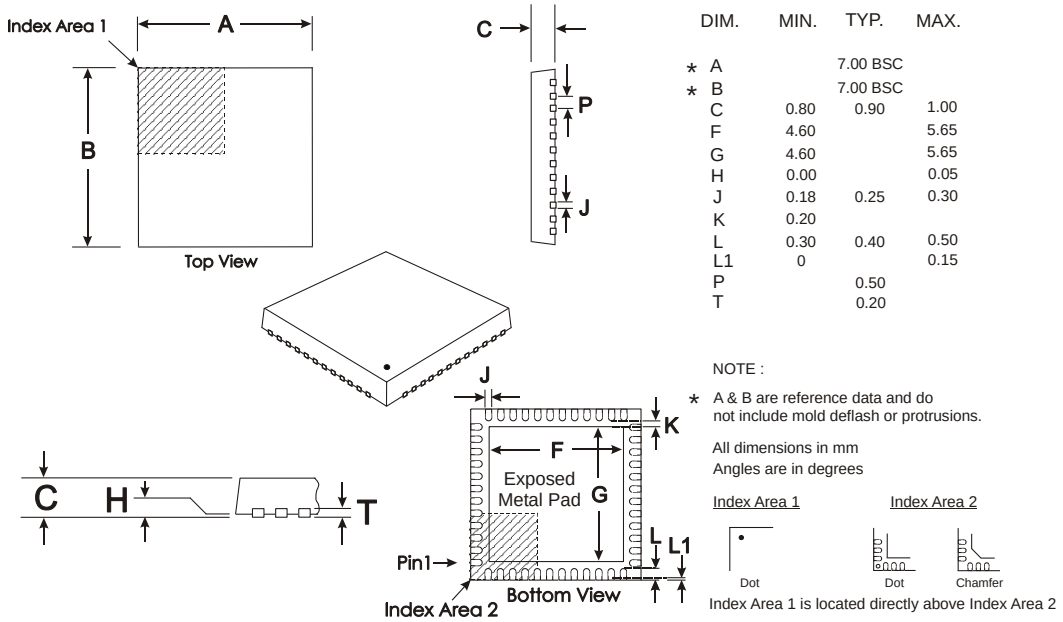
Figure 25 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCL high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable time		0.0	–	–	ns
t_{HIZ}	CSN high to R DATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA set-up time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA set-up time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats, C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7143 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

9.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

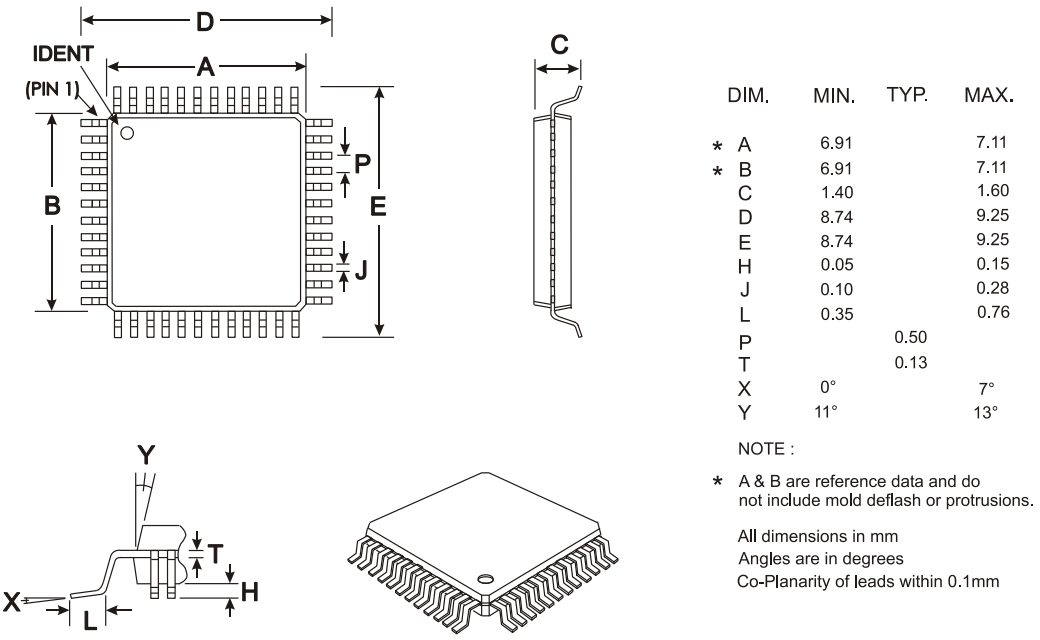
Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 26 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7143Q3



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 27 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7143L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

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CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	CML Microcircuits (USA) Inc. COMMUNICATION SEMICONDUCTORS	CML Microcircuits (Singapore) Pte Ltd COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 62 888129 **Fax:** +65 62 888230 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com
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