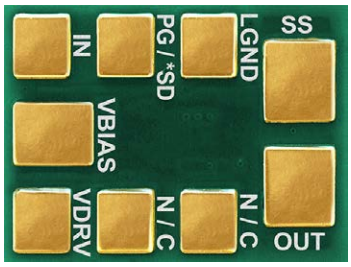
Features

- **Compatible with ALL EPC Space Discrete eGaN® FBG and FDA Series HEMTs**
- **Single Independent eGAN® Gate Driver**
- **Capable of Driving 5000 pF+ Loads**
- **Logic-Compatible Input**
- Gate Bias UVLO Protection, Sensing & Reporting
- Bidirectional Shutdown Input/Power Good Output
- **Internal V_{BIAS} Overvoltage Protection**
- **Fast Transition Times: 30 ns, typ.**
- **High Speed Capability: 3.0 MHz+**
- All eGaN® Switching Elements
- Integrated Driver Bypass Capacitor
- No Bipolar Technology
- Rugged-Molded SMT Package "Pillar" I/O Pads
- Compact 0.500 x 0.375 x 0.135" Size
- -40°C to +85°C Operational Range
- Commercial Screen

Application

- Development Module for FBS-GAM01P-R-PSE
- High Speed DC-DC Conversion
- Synchronous Rectification
- Power Switches/Actuators
- Multi-Phase Motor Drivers



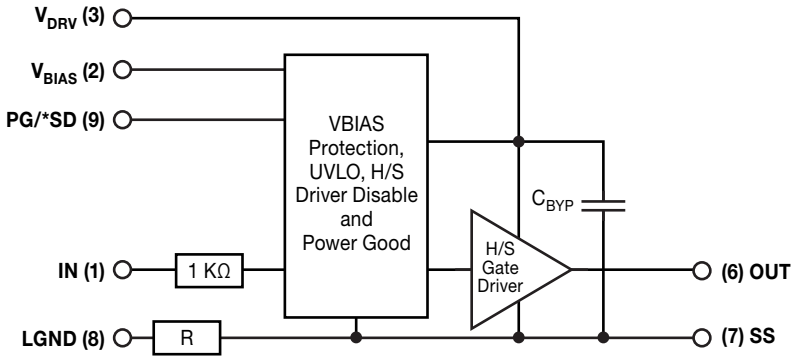
FBS-GAM01P-C-PSE

Single Output eGaN® Gate Driver Development Module

Description

EPC Space's "GaN Driving GaN Technology" **FBS-GAM01P-C-PSE Single Output eGaN® Gate Driver Development Module** integrates a high-speed gate drive circuit consisting entirely of eGaN® switching elements, +5 V_{DC} Input V_{BIAS} under voltage monitoring and reporting, and internal output load gate bias over-voltage clamping protection within an innovative, space-efficient, 9 pin SMT over-molded epoxy package. The FBS-GAM01P-C-PSE provides an excellent engineering development platform transition to the FBS-GAM01P-R-PSE flight version. Circuit design under US Patent #10,122,274 B2, Export Commerce Controlled EAR-99

FBS-GAM01P-C-PSE Functional Block Diagram

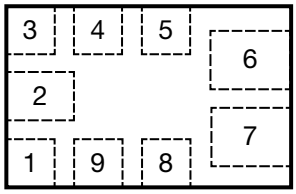


(Pins 4 and 5 are No Connect)

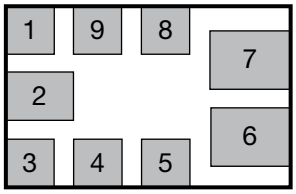
FBS-GAM01P-C-PSE Functional Block Diagram

9 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



FBS-GAM01P-C-PSE Configuration and Pin Assignment Table

Pin #	Pin Name	Input/Output	Pin Function
1	IN	|	Gate Driver Logic Input
2	V_{BIAS}	--	+5 V_{DC} Gate Driver Power Supply Bias Input Voltage
3	V_{DRV}	--	Protected Gate Driver Power Supply Bias Input Voltage
4	N/C	--	No Internal Connection
5	N/C	--	No Internal Connection
6	OUT	O	Gate Drive Output (High Peak Current)
7	SS	--	Source Sense Return/Ground: 0 V (High Peak Current)
8	LGND	--	Logic Return/Ground
9	PG/*SD	I/O	Power Good Output/Shutdown Input

Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions		Value	Units
V_{BIAS}	Gate Driver Bias Supply Voltage	DC	-0.3 to 6	V
		50 ms	7.5	
IN	Logic Input Voltage		-0.3 to 5.5	
T_{STG}	Storage Junction Temperature Range		-55 to +140	°C
T_J	Operating Junction Temperature Range		-40 to +115	
T_C	Case Operating Temperature Range		-40 to +85	
T_{sol}	Package Mounting Surface Temperature		230	
ESD	ESD Class Level (HBM)		1A	

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JC}$	Thermal Resistance Case-to-Ambient (Note 3)	40	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case (Note 3)	11.5	

OUT Static Electrical Characteristics (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
OUT Low-Level Voltage	V_{OL}	V_{BIAS} = 5 V_{DC}, IN = 0.8 V_{DC}, I_{OUT} = 50 µA	T_C = 25°C	-	0.05	0.1	V
			T_C = 40°C T_C = 85°C	- -	0.05 0.1	0.15	
OUT High-Level Voltage	V_{OL}	V_{BIAS} = 5 V_{DC}, IN = 3 V_{DC}, I_{OUT} = -50 µA	T_C = 25°C	4.90	4.95		
			T_C = 40°C T_C = 85°C	 4.85	4.90 4.90	5	
OUT Pull-Down ON-State Resistance (V_{DRV}-OUT)	$R_{DS(on)}$	V_{BIAS} = 5 V_{DC}, IN = 0.8 V_{DC}, I_{OUT} = 0.25 A (Notes 1,2,3)	T_C = 25°C	-	2.5	3.6	Ω
			T_C = 85°C	-	3.8	9	
OUT Pull-Up ON-State Resistance (V_{OUT}-SS)	$R_{DS(on)}$	V_{BIAS} = 5 V_{DC}, IN = 3 V_{DC}, I_{OUT} = -0.25 A (Notes 1,2,3)	T_C = 25°C	-	2.5	3.6	
			T_C = 85°C	-	3.8	9	

IN Logic Input Static Electrical Characteristics (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Low Logic Level Input Voltage	V_{IL}	V_{BIAS} = 5 V_{DC} (Note 4)			0.8	V
High Logic Level Input Voltage	V_{IH}	V_{BIAS} = 5 V_{DC} (Note 5)	2.9			V
Low Logic Level Input Current	I_{IL}	V_{BIAS} = 5 V_{DC}, V_{IL} = 0.4 V_{DC}	-5	+/-1	5	µA
High Logic Level Input Current	I_{IH}	V_{BIAS} = 5 V_{DC}, V_{IH} = 3 V_{DC}	-5	+/-1	5	µA

V_{BIAS} Static Electrical Characteristics (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} Recommended Operating Voltage Range	V_{BIAS}		4.75	5.05	5.25	V
V_{BIAS} Static Operating Current	I_{BIAS}	V_{BIAS} = 5.5 V_{DC}		6.5	10.5	mA

OUT Power Switch Dynamic Electrical Characteristics (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
IN-to-OUT Turn-ON Delay Time	$t_{d(on)}$	V_{BIAS} = 5 V_{DC}; C_{OUT} = 2200 pF (See Switching Figures)			30		ns
IN-to-OUT Turn-OFF Delay Time	$t_{d(off)}$				30		ns
OUT Rise Time	t_r	V_{BIAS} = 5 V_{DC} (See Switching Figures)	C_{OUT} = 1000 pF		32		ns
			C_{OUT} = 2200 pF		49		
			C_{OUT} = 5000 pF		71		
OUT Fall Time	t_f		C_{OUT} = 1000 pF		21		ns
			C_{OUT} = 2200 pF		33		
			C_{OUT} = 5000 pF		55		

Module Static and Dynamic Electrical Characteristics (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Dynamic Gate Driver Losses	P_{GD}	V_{BIAS} = 5 V_{DC}		16		mW/MHz
LGND-SS Resistance	R_s			1		Ω
Minimum Switching Frequency	f_s	V_{BIAS} = 5 V_{DC}; C_{OUT} = 2200 pF (Note 3)	0			Hz
Maximum Switching Frequency	f_s			3.0		MHz

PG Functional Static Electrical Characteristics *(-40°C ≤ T_C ≤ 85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} UVLO Rising Threshold	UVLO+	(Notes 6, 7, 8, 9)			4.70	V
V_{BIAS} UVLO Falling Threshold	UVLO-		2.95			
V_{BIAS} UVLO Hysteresis	(UVLO+) - (UVLO-)			0.15		

PG/*SD Logic I/O Static Electrical Characteristics *(-40°C ≤ T_C ≤ 85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
PG Low Logic Level Output Voltage	V_{OL}	V_{BIAS} = 5 V_{DC} (Notes 6, 7 and 8)			0.2	V
PG High Logic Level Output Voltage	V_{OH}	V_{BIAS} = 5 V_{DC} (Notes 6, 7 and 8)	3.5			V
PG Low Logic Level Output Current	I_{OL}	V_{BIAS} = 5 V_{DC} (Note 6)			10	mA
PG High Logic Level Output Leakage Current	I_{OH}	V_{BIAS} = 5.5 V_{DC} (Note 6)		100		µA
SD Low Logic Level Input Voltage	V_{IL}	V_{BIAS} = 5 V_{DC} (Notes 3, 6, 10)			0.4	V

Specification Notes

1.) V_{BIAS} = +5 V_{DC}, PGND = LGND = 0 V.

2.) Measured using 4-Wire (Kelvin) sensing techniques.

3.) Guaranteed by design. Not tested in production.

4.) When the logic input (IN) is at the low input voltage level the output (OUT) is guaranteed to be OFF (~SS potential).

5.) When the logic input (IN) is at the high input voltage level the output (OUT) is guaranteed to be ON (~V_{DRV} potential).

6.) PG/*SD is bidirectional input/output pin: It is a Shutdown input when pulled to LGND using an open-drain/collector; and it is a Power Good output referenced to LGND. For either the PG or SD function, this pin should be pulled up to V_{DRV} with a 4.7 kΩ resistor.

7.) Parameter measured with a 4.7 kΩ pull-up resistor between PG and V_{DRV}.

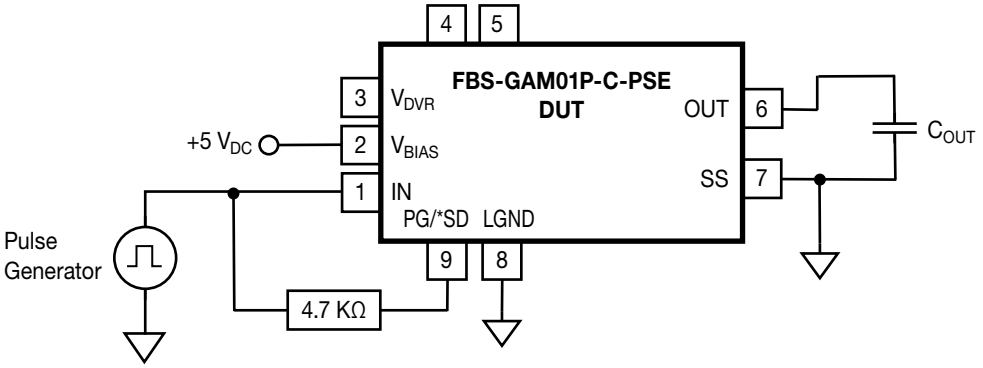
8.) PG is at a low level when V_{BIAS} is below the UVLO- (falling) threshold level and PG is at a high level when V_{BIAS} is above the UVLO+ (rising) threshold level.

9.) V_{BIAS} levels below the UVLO- threshold result in the gate driver being disabled: The logic input to the driver is internally set to a logic low state to prevent damage to the external power eGaN HEMT switch.

10.) When the PG/*SD pin is at the low input voltage level the output (OUT) is guaranteed to be OFF (~SS potential) regardless of the state of the logic input (IN).

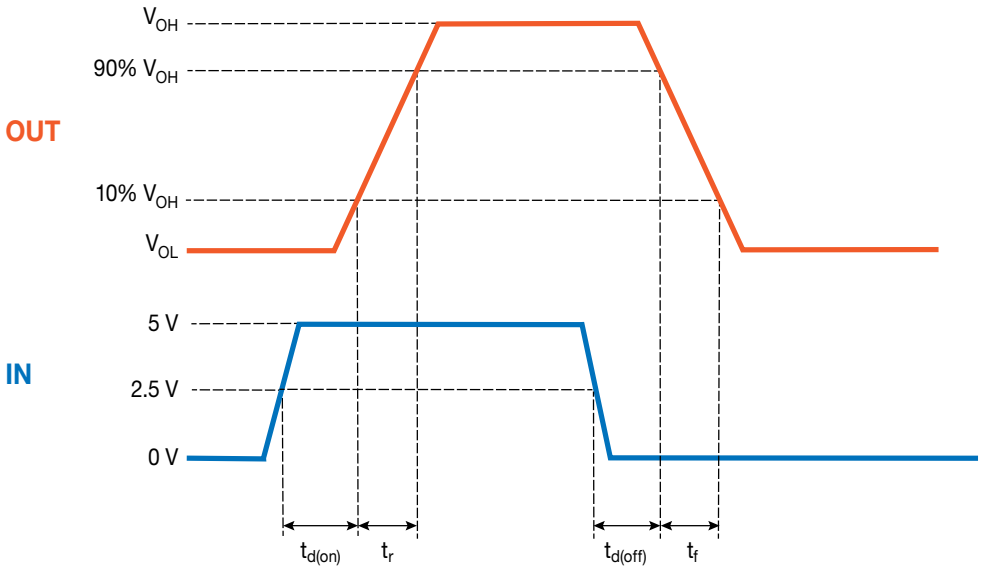
11.) There is a slight offset of the peak output voltage (V_{OH}) from the value of V_{BIAS}. The objective of driving an eGAN® HEMT is to provide sufficient gate drive voltage to ensure that the device is fully enhanced. This value is 5 V_{DC} for EPC Space HEMT devices. Please refer to Figure 5 for the relationship between V_{BIAS} and V_{OH}.

Switching Figures



Only pins connected during testing identified.
Pulse Generator set to 1 MHz frequency, 50% duty cycle.

Figure 1. IN-to-OUT Switching Time Test Circuit



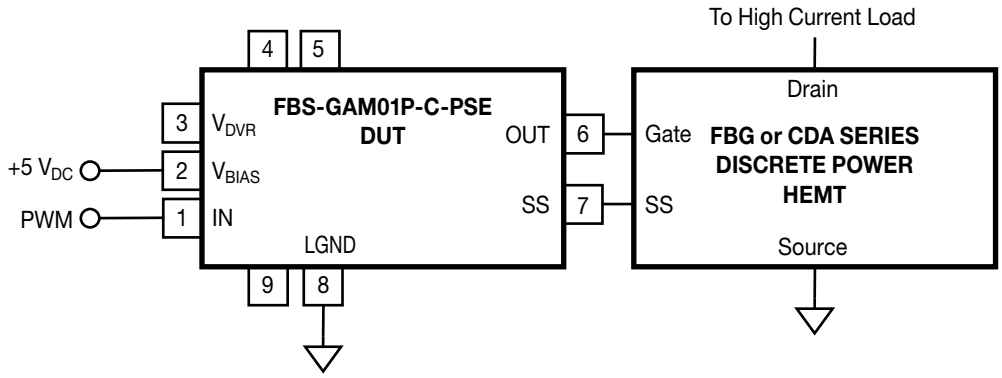
NOTE: Waveforms exaggerated for clarity and observability.

Figure 2. IN-to-OUT Switching Time Definition

Typical Application Information

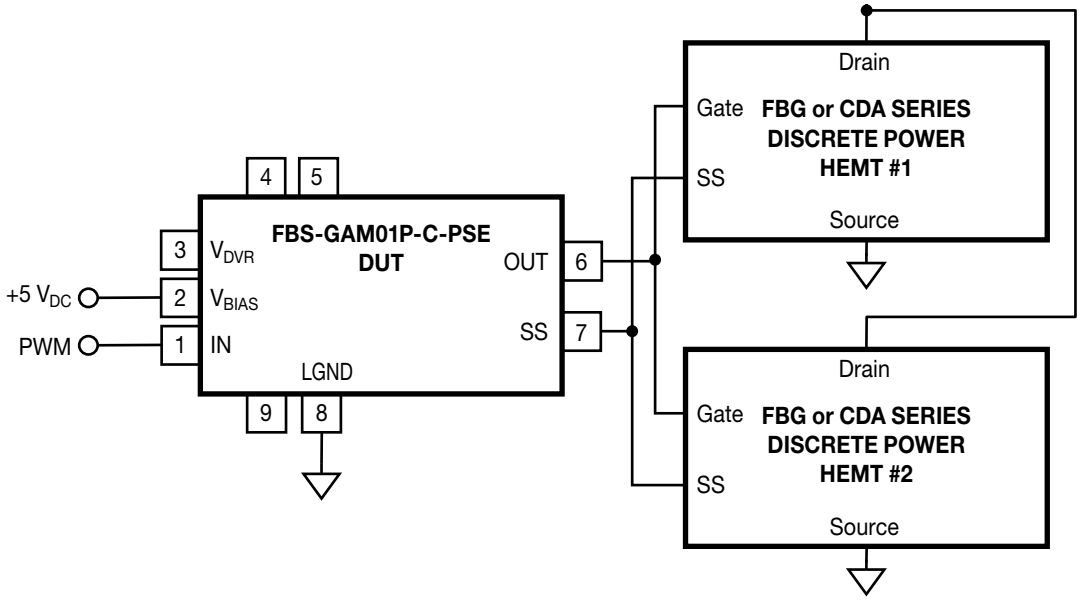
The following figures detail the suggested applications for the FBS-GAM01P-C-PSE Module. For all applications, please refer to the following sections for proper power supply bypassing and layout recommendations and criteria.

In all the following figures, only the pins that are considered or that require connection are identified.



Note: Keep Out-Gate and Source-Sense-SS connections as short as possible.

Figure 3. Driving Single EPC Space eGaN® HEMT



Note: Make all Out-Gate and SS-SS connections of equal length and as short as possible. Make all HEMT Source connections as short as possible and make all HEMT Drain connections as equal length as possible.

Figure 4. Driving Multiple EPC Space eGaN® HEMTs

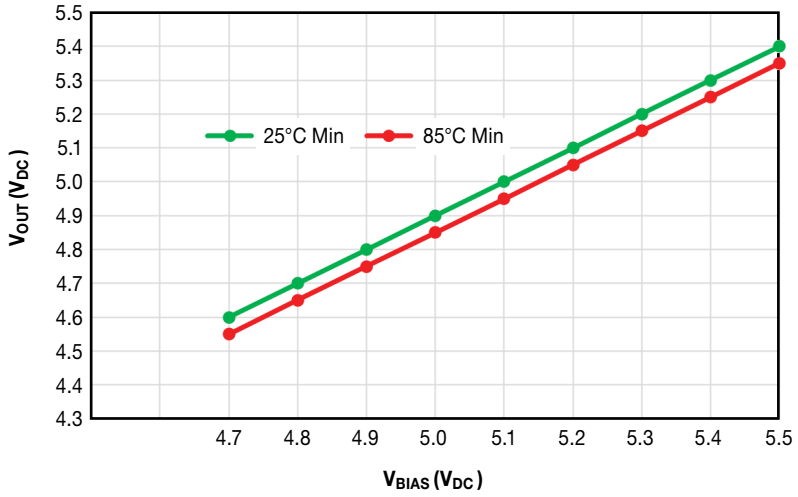


Figure 5. V_{OUT} to V_{BIAS} Relationship

Pin Descriptions

IN (Pin 1)

The IN pin is the logic input for the gate driver. When the IN input pin is logic low ("0"), the OUT pin is in the low (~0 V) state. When the IN pin is logic high ("1"), the OUT pin is in the high (~V_{DRV}) state, measured with respect to SS.

V_{BIAS} (Pin 2)

The V_{BIAS} pin is the raw input DC power input for the FBS-GAM01P-C-PSE. It is recommended that a 1.0 microfarad ceramic capacitor and a 0.1microfarad ceramic capacitor, each 25 V_{DC} rating, be connected between V_{BIAS} (pin 2) and Source Sense (pin 7) to obtain the specified switching performance.

V_{DRV} (Pin 3)

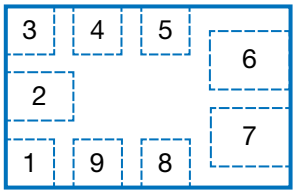
The V_{DRV} pin (Pin 3) of the FBS-GAM01P-C-PSE is the protected V_{BIAS} power supply for the high-speed gate driver for the external eGaN® power HEMT. This is a test pin for the module. Unless otherwise directed in this specification, this pin should be left **open** for proper operation of the module.

N/C (Pins 4 and 5)

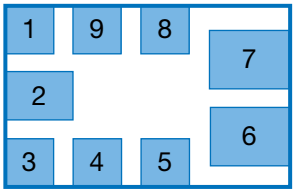
Pins 4 and 5 are not internally connected. These internal "no connection" pins are recommended to be grounded to the system power ground/return as good engineering practice to avoid coupling unwanted noise into the internal circuitry of the FBS-GAM01P-C-PSE, either directly or via 0 Ω jumper resistors.

9 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



Pin Descriptions *(continued)*

OUT (Pin 6)

The OUT pin (pin 6) is the high peak current output pin that connects to the corresponding GATE pin on all EPC Space power eGaN® HEMT packages or to the gate connection of an external power eGaN® HEMT. To minimize series inductance, and thus gate voltage overshoot during switching transients, keep the connection between the OUT pin and the external HEMT gate pin as short as possible, and preferably on the same PCB etch layer.

SS (Pin 7)

The SS pin (pin 6) is the "Source Sense," high peak current return pin that connects to the corresponding SS pin on all EPC Space power eGaN® HEMT packages. To minimize series inductance, and thus gate voltage overshoot during switching transients, keep the connection between the OUT pin and the external HEMT gate pin as short as possible, and preferably on the same PCB etch layer. In the case where the FBS-GAM01P-C-PSE is driving an external HEMT that does not have an SS pin, the SS pin (pin 7) on the module should be connected as close as possible to the Source connection on the external HEMT. Please note that uncontrolled gate voltage overshoots may be encountered due to common source inductance in this situation.

LGND (Pin 8)

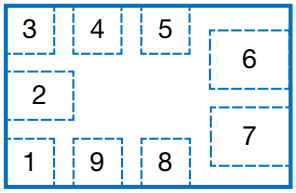
Logic ground for the module. For proper operation of the FBS-GAM01P-C-PSE, the LGND pin (Pin 8) MUST be connected directly to the system logic ground return in the application circuit.

PG/*SD (Power Good Output/Shutdown Input) (Pin 9)

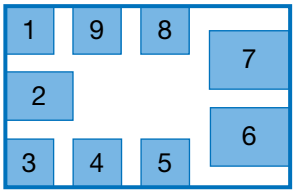
The bidirectional Power Good (PG) output and Shutdown (*SD) input pin. To externally disable the FBS-GAM01P-C-PSE (with the OUT pin forced to the low (OFF) state), the SD/PG pin should be connected to logic ground, such as via an open-drain/collector. The module also incorporates a Power Good (PG) sensing circuit that disables the driver when the +5 V_{DC} gate drive bias potential (V_{BIAS}) falls below an under-voltage threshold range as specified in the Table "PG Functional Static Electrical Characteristics" (See Page 4). During the time when the V_{BIAS} potential is below the pre-set threshold, the PG output (Pin 5) pin is pulled low (to LGND) via an open drain. Alternatively, when the V_{BIAS} potential is above the pre-set threshold the PG pin is pulled high via an external pull up resistor to V_{DRV}. For proper operation, pin 9 should be externally pulled-up to V_{DRV} (pin 3) with a 4.7 kΩ resistor.

9 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



DC Operation and Power Up Sequencing

The recommended power sequencing for the FBS-GAM01P-C-PSE is the VBIAS power supply is applied first and within the recommended operating voltage range prior to the application of V_{DD} to the circuit. The FBS-GAM01P-C-PSE is designed as a switching eGAN® HEMT driver that is inherently capable of DC (steady-state) operation. As such, there are precautions that must be observed during the application and operation of this Module. One of these precautions is power-up sequencing. The power MUST be sequenced to the circuit with V_{BIAS} being applied first and within its recommended operating voltage range before V_{DD} is applied to the circuit. This will prevent the gate driver output (OUT) from assuming a non-deterministic state with regards to the logic input (IN) and unintentionally providing an internal drive signal to the internal eGaN® HEMT power switch(es). Under NO circumstances should an FBS-GAM01P-C-PSE Module be used in a half-bridge configuration with V_{DD} applied first, prior to VBIAS, to the Module.

Regardless, the EPC Space recommended power sequencing for the FBS-GAM01-C-PSE is V_{BIAS} is applied first and within the recommended operating voltage range prior to the application of V_{DD} to the circuit.

Suggested FBS-GAM01P-C-PSE Schematic Symbol

The suggested schematic symbol for the FBS-GAM01P-C-PSE is shown in Figure 6. This symbol groups the I/O pins of the FBS-GAM01P-C-PSE into groups of similar functionality.

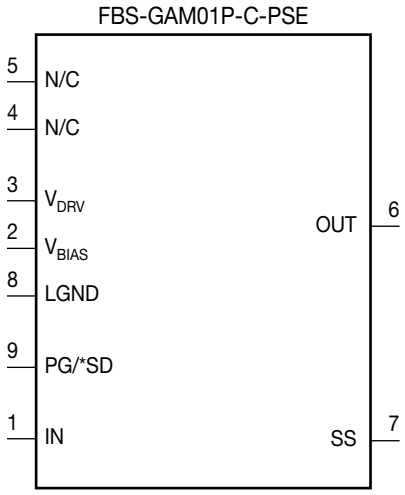
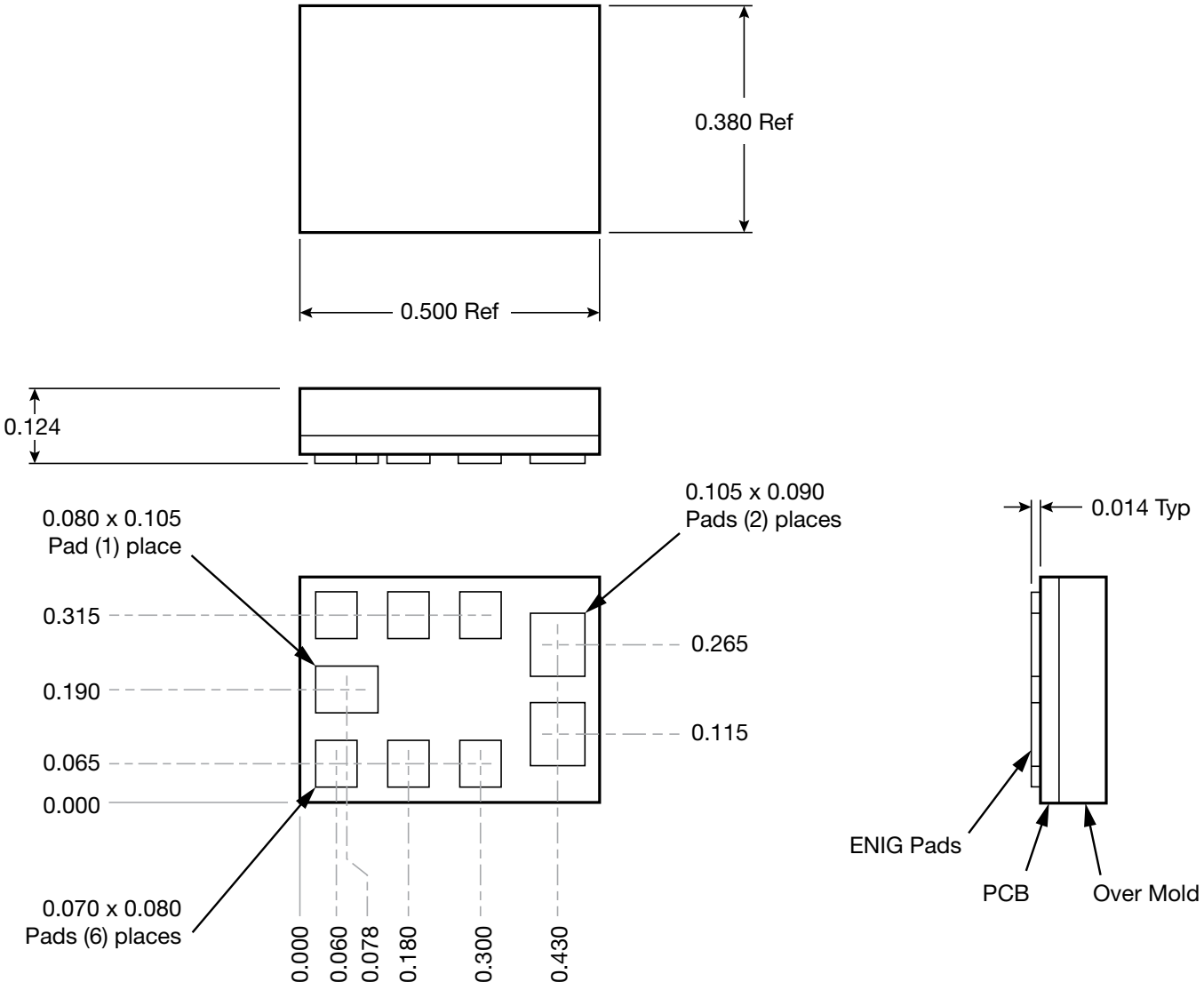


Figure 6. Suggested FBS-GAM01P-C-PSE Schematic Symbol

Package Outline and Dimensions



Note: All dimensions are in inches
ALL tolerances +/- 0.010

Figure 7. FBS-GAM01P-C-PSE Package Outline and Dimensions

Recommended PCB Solder Pad Configuration

The novel I/O "pillar" pads fabricated onto the bottom surface of the FBS-GAM01P-C-PSE module are designed to provide optimal electrical, thermal and mechanical properties for the end-use system designer. To achieve the full benefit of these properties, it is important that the FBS-GAM01P-C-PSE module be soldered to the PCB motherboard using SN63 (or equivalent) solder. The recommended pad dimensions and locations are shown in Figure 8. All dimensions are shown in inches.

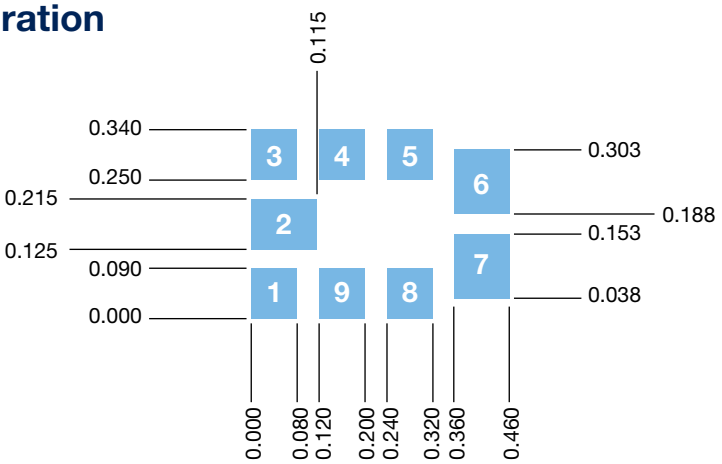


Figure 8. Recommended PCB Solder Pad Configuration (Top View)

Sn63/Pb37 No Clean Solder Paste Typical Example Profile

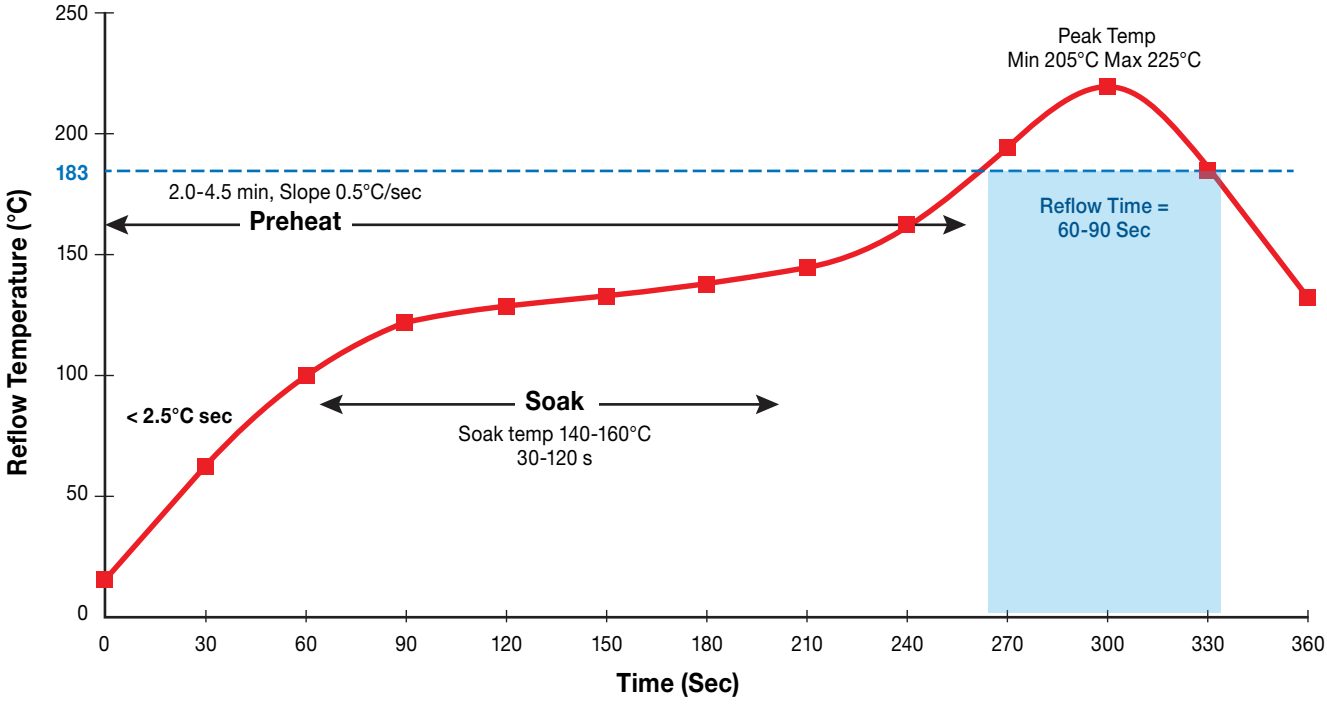


Figure 9. Sn63/Pb37 No Clean Solder Paste Typical Reflow Example Profile

Preheat Zone – The preheat zone, is also referred to as the ramp zone, and is used to elevate the temperature of the PCB to the desired soak temperature. In the preheat zone the temperature of the PCB is constantly rising, at a rate that should not exceed 2.5°C/sec. The oven's preheat zone should normally occupy 25-33% of the total heated tunnel length.

The Soak Zone – normally occupies 33-50% of the total heated tunnel length exposes the PCB to a relatively steady temperature that will allow the components of different mass to be uniform in temperature. The soak zone also allows the flux to concentrate and the volatiles to escape from the paste.

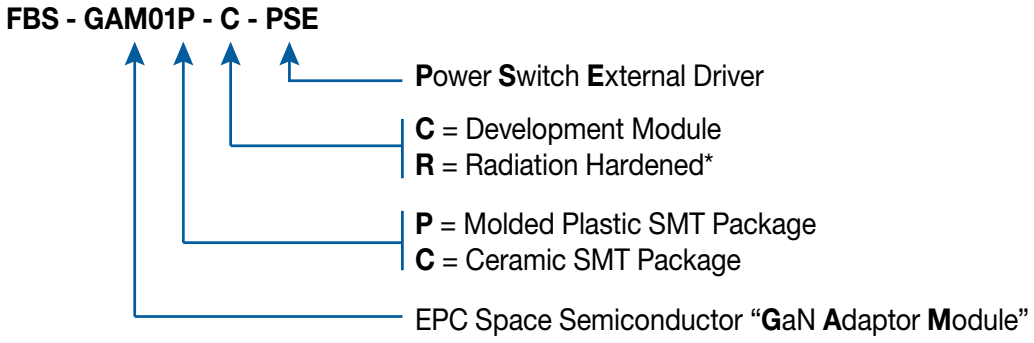
The Reflow Zone – or spike zone is to elevate the temperature of the PCB assembly from the activation temperature to the recommended peak temperature. The activation temperature is always somewhat below the melting point of the alloy, while the peak temperature is always above the melting point.

Reflow – Best results are achieved when reflowed in a forced air convection oven with a minimum of 8 zones (top & bottom), however reflow is possible with a 4 Zone oven (top & bottom) with the recommended profile for a forced air convection reflow process. The melting temperature of the solder, the heat resistance of the components, and the characteristics of the PCB (i.e. density, thickness, etc.) determine the actual reflow profile.

Note: FBS-GAM01P-C-PSE solder attachment has a maximum 230°C peak dwell temperature limit, exceeding the maximum peak temperature can cause damage the unit.

Reflow Disclaimer – The profile is as stated as an "Example" – the end user can optimize profiling based against the actual solder paste used -- EPC Space assumes no liability in conjunction with the use of this profile information.

EPC Space Part Number Information



* FBS-GAM01P-R-PSE (Utilizes High Lead Content Die) and
FBS-GAM01C-R-PSE (Utilizes High Lead Content Die)

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The products described in this datasheet could be subjected to the International in Arms Regulations (ITAR). They require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Patents

EPC Space holds numerous U.S and international patents. US Patent #10,122,274 B2, 15/374,756, 15/374,774, PCT/US2016/065952, PCT/US2016/065946. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with U.S Patent laws

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Revisions

Datasheet Revision	Product Status
REV -	Proposal/development
M-702-004-Q7	Characterization and Qualification
	Production Released

Information subject to change without notice.
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