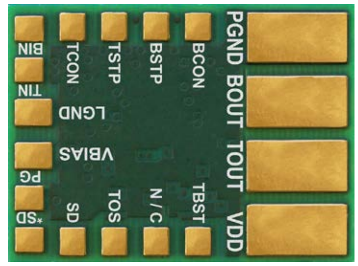
FBS-GAM02P-C-PSE

Features

- 50 V_{DC} Fully De-Rated Operation (100 V_{DC} Capable)
- Internal 100 V-Rated Bootstrap Diode
- Independent Low and High Side eGaN® HEMT Gate Drivers
- Four Possible Configurations:
  - Single Low-Side Gate Driver
  - Single High-Side Gate Driver
  - Independent Low- and High-Side Gate Drivers
  - Half-Bridge Gate Drivers with Input Shoot-through Protection
- Internal Power Good Circuitry
- High Speed Switching Capability: 1.0+ MHz
- Rugged Compact Molded SMT Package
- “Pillar” I/O Pads
- Compact Package Size: 1.00 x 0.75 x 0.125”
- **Drives External eGaN® Switching Elements**
- No Bipolar Technology
- Compact 1.00 x 0.75 x 0.125” Size
- -40°C to +85°C Operational Range
- Commercial Screen

Application

- **Development Platform for FBS-GAM02P-R-PSE**
- Power Switches/Actuators
- Single and Multi-Phase Motor Phase Drivers
- High Speed DC-DC Conversion



FBS-GAM02P-C-PSE

50 V_{DC} High-Speed Multifunction Power eGaN® HEMT Driver

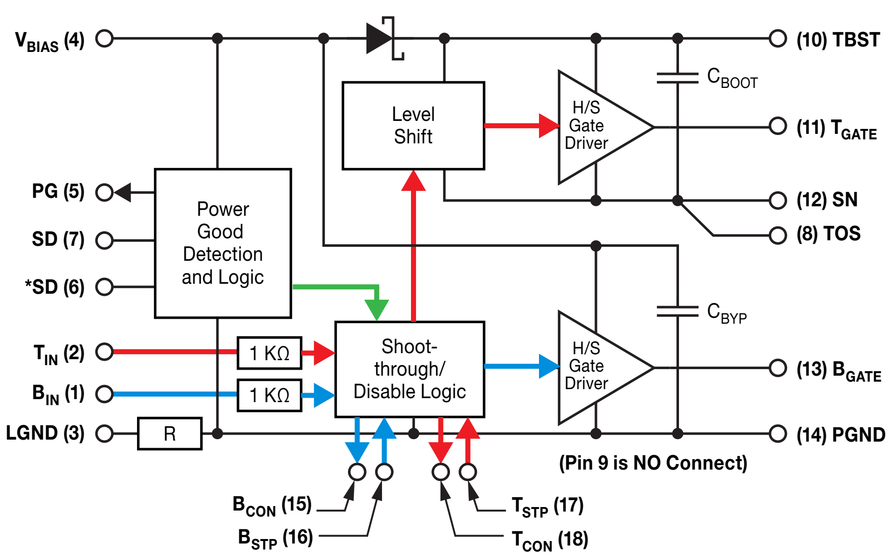
Description

EPC Space’s **FBS-GAM02P-C-PSE** Series **High-Speed Multifunction Power Gate Driver Development Module** incorporate eGaN® HEMTs designed with EPC Space’s “GaN-Driving-GaN Patented Technology.” The modules contain ***two independent high-speed gate drive circuits*** (consisting entirely of eGaN® switching elements), a high-side driver bootstrap diode, ***input shoot-through prevention*** logic for the half-bridge configuration and +5 V_{DC} gate drive bias ***power good monitoring*** circuitry in an innovative, space-efficient, 18 pin SMT over-molded epoxy package provides for an excellent engineering brass-board development platform for the **FBS-GAM02P-R-PSE** flight unit version. Circuit Design under US Patent #10,122,274 B2.

The FBS-GAM02P-C-PSE is intended to drive external EPC Space eGaN® HEMT power switch transistors rated up to 100 V (refer to Table 1 for device options).

Commerce Rated 9A515.x Device.

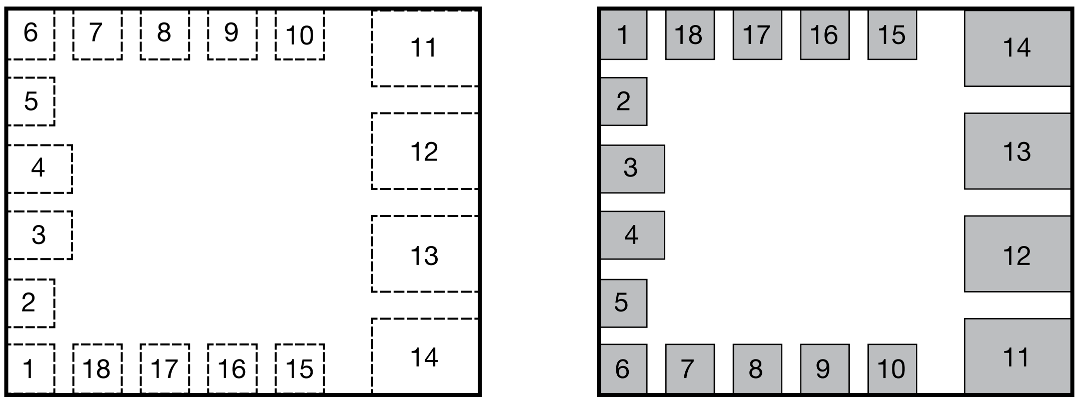
FBS-GAM02P-C-PSE Functional Block Diagram



FBS-GAM02P-C-PSE Functional Block Diagram

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View **Bottom (Pad) View**



FBS-GAM02P-C-PSE Configuration and Pin Assignment Table

Pin #	Pin Name	Input/Output	Pin Function
1	B_{IN}	I	Low-Side Switch Logic Input
2	T_{IN}	I	High-Side Switch Logic Input
3	LGND	--	Logic Ground, 0 V (Low Current)
4	V_{BIAS}	--	+5 V Gate Driver Power Supply Bias Input Voltage
5	PG	O	Power Good Logic Output (Open Drain)
6	*SD	I	Low True Shutdown Input
7	SD	I	High True Shutdown Input
8	TOS	--	Switching Node Sense
9	N/C	--	No Internal Connection
10	TBST	--	High-Side Bootstrap Potential
11	T_{GATE}	O	High-Side Gate Output
12	SN	--	High-Side Switching Node*
13	B_{GATE}	O	Low-Side Gate Output
14	PGND	--	Power Supply Return, 0 V
15	B_{CON}	I	Low-Side Switch Control Input
16	B_{STP}	O	Low-Side Switch Shoot Through Protection Output
17	T_{STP}	O	High-Side Switch Shoot Through Protection Output
18	T_{CON}	I	High-Side Switch Control Input

* High-Side HEMT Gate Driver Reference Potential. Connect to Source Sense (SS) of External High-Side Power HEMT.

Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Value	Units
SN to PGND	High Side Gate Driver Reference Voltage (Note 1)	50	V
C_{OUT}	B_{GATE} or T_{GATE} Output Capacitance	10,000	pF
V_{BIAS}	Gate Driver Bias Supply Voltage	-0.3 to 6.5	V
B_{IN}, T_{IN}	B_{IN} or T_{IN} Input Voltage	-0.3 to 5.0	
T_{STG}	Storage Junction Temperature Range	-55 to +140	°C
T_J	Operating Junction Temperature Range	-40 to +130	
T_c	Case Operating Temperature Range	-40 to +85	
T_{sol}	Package Mounting Surface Temperature	225	
ESD	ESD class level (HBM)	1A	

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta CA}$	Thermal Resistance Case-to-Ambient (Note 3)	28	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case (Note 3)	11	

B_{GATE}, T_{GATE} Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
B_{GATE} – PGND Low Level Voltage	V_{OL}	V_{BIAS} = 5 V_{DC}, PGND = 0 V_{DC}, B_{IN} = 0.8 V_{DC}, I_{BGATE} = 50 µA	T_C = 25°C	-	0.05	0.10	V_{DC}
			T_C = 85°C	-	0.10	0.15	
			T_C = -40°C	-	0.10	0.15	
B_{GATE} – PGND High Level Voltage	V_{OH}	V_{BIAS} = 5 V_{DC}, PGND = 0 V_{DC}, B_{IN} = 3 V_{DC}, I_{BGATE} = -50 µA	T_C = 25°C	4.90	4.95		V_{DC}
			T_C = 85°C	4.80	4.85		
			T_C = -40°C	4.80	4.85		
T_{GATE} – SN Low Level Voltage	V_{OL}	V_{BIAS} = 5 V_{DC}, SN = PGND = 0 V_{DC}, T_{IN} = 0.8 V_{DC}, I_{TGATE} = 50 µA	T_C = 25°C	-	0.05	0.10	V_{DC}
			T_C = 85°C	-	0.10	0.15	
			T_C = -40°C	-	0.10	0.15	
T_{GATE} – SN High Level Voltage	V_{OH}	V_{BIAS} = 5 V_{DC}, SN = PGND = 0 V_{DC}, T_{IN} = 3 V_{DC}, I_{TGATE} = -50 µA	T_C = 25°C	4.45	4.55		V_{DC}
			T_C = 85°C	5.10	5.15		
			T_C = -40°C	4.25	4.30		
B_{GATE} – PGND Pull-Down ON-State Resistance	$R_{DS(on)}$	V_{BIAS} = 5 V_{DC}, B_{IN} = 0.8 V_{DC}, I_{BGATE} = 0.25 A (Notes 3, 4)	T_C = 25°C	-	2.5	3.5	Ω
			T_C = 85°C	-	4.5	6.0	
			T_C = -40°C	-	1.3	2.0	
B_{GATE} – PGND Pull-Up ON-State Resistance	$R_{DS(on)}$	V_{BIAS} = V_{BIAS} = 5 V_{DC}, B_{IN} = 3 V_{DC}, I_{BGATE} = -0.25 A (Notes 3, 4)	T_C = 25°C	-	2.5	3.5	Ω
			T_C = 85°C	-	4.5	6.0	
			T_C = -40°C	-	1.3	2.0	
T_{GATE} – SN Pull-Down ON-State Resistance	$R_{DS(on)}$	V_{BIAS} = V_{BST} = 5 V_{DC}, PGND = SN = 0 V_{DC}, T_{IN} = 0.8 V_{DC}, I_{TGATE} = 0.25 A (Notes 3, 4)	T_C = 25°C	-	2.5	3.5	Ω
			T_C = 85°C	-	4.5	6.0	
			T_C = -40°C	-	1.3	2.0	
T_{GATE} – SN Pull-Up ON-State Resistance	$R_{DS(on)}$	V_{BIAS} = V_{BST} = 5 V_{DC}, PGND = SN = 0 V_{DC}, T_{IN} = 3 V_{DC}, I_{TGATE} = -0.25 A (Notes 3, 4)	T_C = 25°C	-	2.5	3.5	Ω
			T_C = 85°C	-	4.5	6.0	
			T_C = -40°C	-	1.3	2.0	

B_{IN}, T_{IN} Logic Input Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Low Logic Level Input Voltage	V_{IL}	V_{BIAS} = 5 V_{DC} (Note 5)				0.8	V
High Logic Level Input Voltage	V_{IH}	V_{BIAS} = 5 V_{DC} (Note 6)		2.9			V
Low Logic Level Input Current	I_{IL}	V_{BIAS} = 5 V_{DC}, V_{IL} = 0.4 V	T_C = 25°C	-5	+/-1	+5	µA
			T_C = 85°C	-30	+/-10	30	
High Logic Level Input Current	I_{IH}	V_{BIAS} = 5 V_{DC}, V_{IL} = 3 V	T_C = 25°C	-5	+/-1	+5	µA
			T_C = 85°C	-30	+/-10	30	

SN-to-PGND Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
SN-PGND Leakage Current (Notes 1,2,3)	I_L	SN = 50 V_{DC}, T_{IN} = 0.8 V_{DC}, V_{BIAS} = 5 V_{DC}, PGND = 0 V_{DC}		1.5	15	µA
		SN = 20 V_{DC}, T_{IN} = 0.8 V_C, V_{BIAS} = 5 V_{DC}, PGND = 0 V_{DC}		80	15	mA
SN-to-PGND Operating Voltage Range	SN-to-PGND	(Note 3)	5		50	V

V_{BIAS} Static Electrical Characteristics *(-40 < T_C <85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} Recommended Operating Voltage Range	V_{BIAS}	(Note 10)	4.75	5.2	5.25	V
V_{BIAS} Operating Current	I_{BIAS}	V_{BIAS} = 5.25 V_{DC}		16	20	mA

PG Logic Output Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Low Logic Level Output Voltage	V_{OL}	V_{BIAS} = 5 V_{DC} (Notes 7, 8)			0.2	V
High Logic Level Output Voltage	V_{OH}	V_{BIAS} = 5 V_{DC} (Notes 7, 8)	3.5			V
Low Logic Level Output Current	I_{OL}	V_{BIAS} = 5 V_{DC} (Notes 7, 9)			5	mA
High Logic Level Output Leakage Current	I_{OH}	V_{BIAS} = 5.25 V_{DC} (Notes 7, 9)		100		µA

PG Functional Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} UVLO Rising Threshold	UVLO+	(Notes 7, 8, 9,10)			4.7	V
V_{BIAS} UVLO Falling Threshold	UVLO-		2.95			
V_{BIAS} UVLO Hysteresis	UVLO+ - UVLO-			0.2		
V_{BIAS} OVLO Rising Threshold	OVLO+			6.70		
V_{BIAS} OVLO Falling Threshold	OVLO-		5.55			
V_{BIAS} OVLO Hysteresis	OVLO+ - OVLO-			0.12		

OUT Power Switch Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
B_{IN}-to-B_{OUT} Turn-ON Delay Time	$t_{d(on)}$	V_{BIAS} = 5 V_{DC}, PGND = 0 V_{DC}, C_{OUT} = 2200 pF (See Switching Figures)			22	35	ns
B_{IN}-to-B_{OUT} Turn-OFF Delay Time	$t_{d(off)}$				22	35	
B_{IN}-to-B_{OUT} Turn-ON Delay Time	$t_{d(on)}$	V_{BIAS} = TBST = 5 V_{DC}, SN = PGND = 0 V_{DC}, C_{OUT} = 2200 pF (See Switching Figures)			45	60	
B_{IN}-to-B_{OUT} Turn-OFF Delay Time	$t_{d(off)}$				60	75	
B_{GATE} Rise Time	t_r	V_{BIAS} = 5 V_{DC}, PGND = 0 V_{DC}, (See Switching Figures) (Note 4)	C_{OUT} = 1000 pF		8		
			C_{OUT} = 2200 pF		12		
			C_{OUT} = 5000 pF		28		
B_{GATE} Fall Time	t_f		C_{OUT} = 1000 pF		8		
			C_{OUT} = 2200 pF		12		
			C_{OUT} = 5000 pF		28		
T_{GATE} Rise Time	t_r	V_{BIAS} = T_{BST} = 5 V_{DC}, SN = PGND = 0 V_{DC}, (See Switching Figures) (Note 4)	C_{OUT} = 1000 pF		15		
			C_{OUT} = 2200 pF		25		
			C_{OUT} = 5000 pF		40		
T_{GATE} Fall Time	t_f		C_{OUT} = 1000 pF		15		
			C_{OUT} = 2200 pF		25		
			C_{OUT} = 5000 pF		40		

Module Static and Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Dynamic Gate/Driver Losses	P_{GD}	V_{BIAS} = 5 V_{DC}		22	35	ns
B_{GATE} - PGND, T_{GATE} - SN Output Drive Capacitance Range	C_{OUT}			2200	5000	pF
Low Side Gate Driver Duty Cycle Range	D/C		0		100	%
High Side Gate Driver Maximum Switching Frequency	f_s			1.5		MHz
High Side Gate Driver Start Up Pre-Charge Time: Half Bridge Configuration	t_{pcg}	(Notes 3, 10, 11, 12)	5			µs
High Side Gate Driver Minimum Operating Switching Frequency	$f_{sw(min)}$		200			kHz
High Side Gate Driver Duty Cycle Range	$t_{d/c}$		0		95	%
High Side Gate Driver Maximum Switching Frequency	f_s	(Notes 11, 12, 13)		2		MHz
Shoot-Through Protection Activation Delay Time	t_{st}	(Notes 3, 14)		5		ns
Internal Bootstrap Capacitance	C_{boot}	TBST (Pin 10) to TOS (Pin 8)		47		nF
External Bootstrap Capacitance	C_{boot}(ext)				1	µF
LGND – PGND Resistance	R_S			1		Ω

Specification Notes

1.) V_{BIAS} = +5 V_{DC}, PGND = LGND = 0 V_{DC} , B_{IN} = 0 V_{DC} , T_{IN} = 3 V_{DC} and SN = 50 V_{DC}.

2.) Leakage current measured from SN to PGND.

3.) Guaranteed by design. Not tested in production.

4.) f_s = 200 kHz, Duty cycle = 50%.

5.) When either logic input (B_{IN} or T_{IN}) is at the low input voltage level the associated gate drive output (B_{GATE} or T_{GATE}) is guaranteed to be in the LOW state (low impedance to PGND or SN).

6.) When either logic input (B_{IN} or T_{IN}) is at the high input voltage level the associated gate drive output (B_{GATE} or T_{GATE}) is guaranteed to be in the HIGH state (low impedance to V_{BIAS} or TBST).

7.) Parameter measured with a 4.7 kΩ pull-up resistor between PG and V_{BIAS}.

8.) PG is at a low level when V_{BIAS} is below the UVLO falling threshold level or the OVLO rising threshold level. PG is at a high level when V_{BIAS} is above the UVLO rising threshold level or the UVLO rising threshold level. Refer to Figure 5.

9.) PG is an open drain output referenced to PGND/LGND.

10.) V_{BIAS} levels below the UVLO- and above the OVLO+ thresholds result in the low side and high side gate drivers being disabled: The logic inputs to the drivers are internally set to a logic low state (i.e. OFF) to prevent damage to the external EPC Space eGaN® HEMT power switches.

11.) The high side gate driver utilizes a bootstrap capacitor to provide the proper bias for this circuit. As such, this capacitor **MUST** be periodically re-charged from the V_{BIAS} supply. The time t_{pcg} is the minimum time required to ensure that the bootstrap capacitor is properly charged when power is initially applied to the FBS-GAM02P-R- PSE Module.

12.) The minimum frequency of operation is determined by the internal bootstrap capacitance and the bias current required by the high side gate driver circuit.

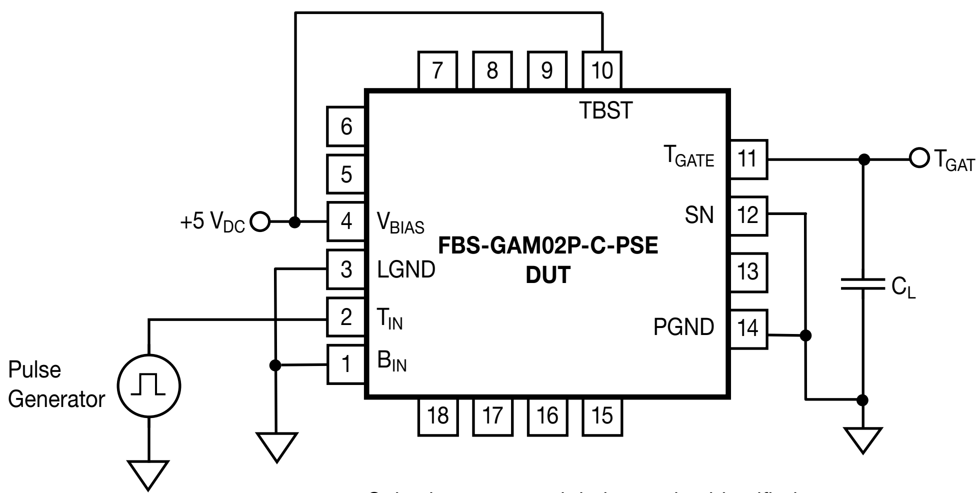
13.) In order to keep the high side gate driver bootstrap capacitor properly charged in switching applications it is recommended that the maximum duty cycle (t_{on}/f_s) of the top power switch is limited to the value shown.

Consequently, the high side gate driver is unsuitable for DC applications, unless an external DC power supply capable of withstanding high dV/dt from input-to-output is provided to the high side gate driver via pins TBST (pin 10) and TOS (pin 8).

14.) The input shoot-through protection is activated if both the B_{IN} and T_{IN} logic inputs are set to the logic high (“1”) condition simultaneously. If the B_{IN} and T_{IN} inputs are activated simultaneously and B_{STP} is connected to B_{CON} and T_{STP} is connected to T_{CON} then both B_{GATE} and T_{GATE} are in the LOW state (i.e. OFF) with respect to, respectively, PGND and SN.

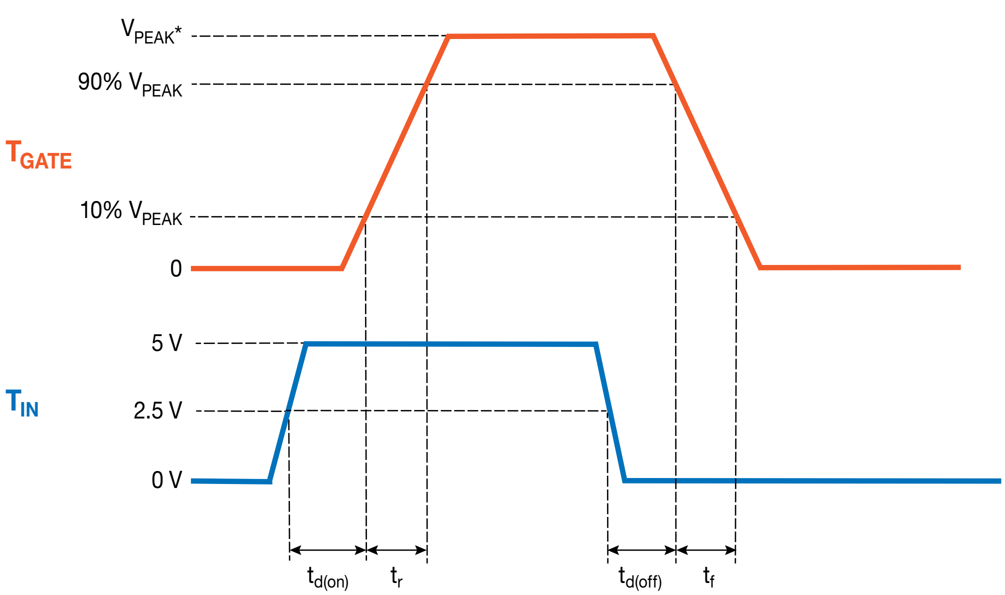
15.) There is a slight offset of the peak output voltage (V_{OH}) from the value of V_{BIAS}. This offset is greater for the high-side gate driver than the low-side gate driver due to the presence of the Schottky bootstrap diode. The objective of driving an eGAN® HEMT is to provide sufficient gate drive voltage to ensure that the device is fully enhanced. This value is 5.0 V_{DC} for EPC Space HEMT devices. Please refer to Figures 6 and 8 for the relationship between V_{BIAS} and V_{OUT} (V_{OH}) for the low- and high-side gate drivers, respectively, for guidance as to where to set V_{BIAS} for optimum performance in the end-application.

Switching Figures



Only pins connected during testing identified.
Pulse Generator set to 500 kHz frequency, 5% duty cycle.

Figure 1. T_{IN}-to-T_{GATE} Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.
* V_{PEAK} is ~V_{BIAS} – 0.3 V_{DC}.

Figure 2. T_{IN}-to-T_{GATE} Switching Time Definition

Switching Figures *(continued)*

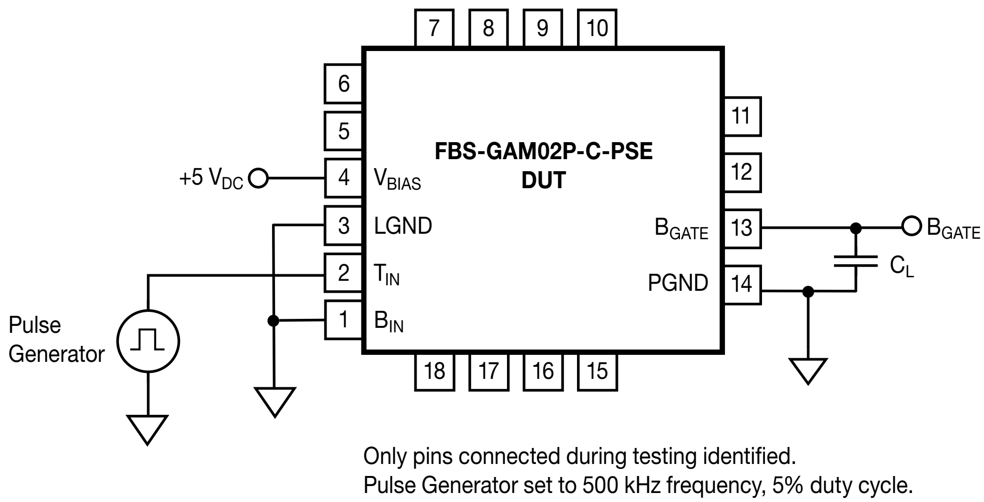
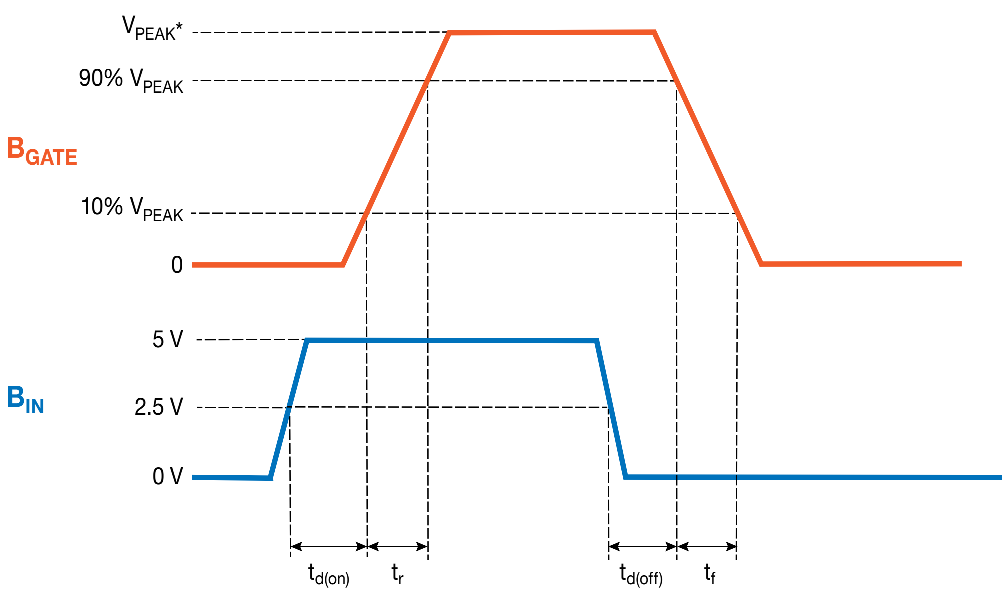


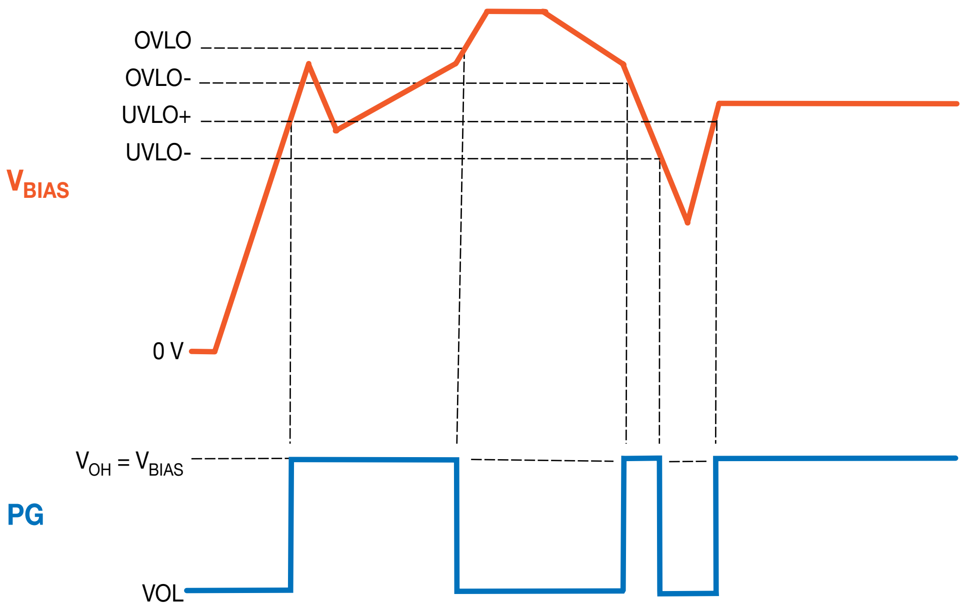
Figure 3. B_{IN}-to-B_{GATE} Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.
* V_{PEAK} is ~V_{BIAS}

Figure 4. B_{IN}-to-B_{GATE} Switching Time Definition

Switching Figures *(continued)*



NOTE: Waveforms exaggerated for clarity and observability.

Figure 5. V_{BIAS}-to-PG Relationship

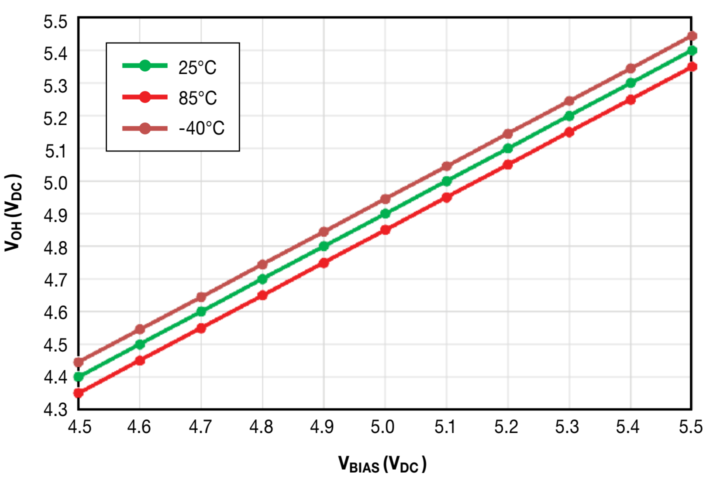


Figure 6. Low-Side V_{OUT}-to-V_{BIAS} Relationship

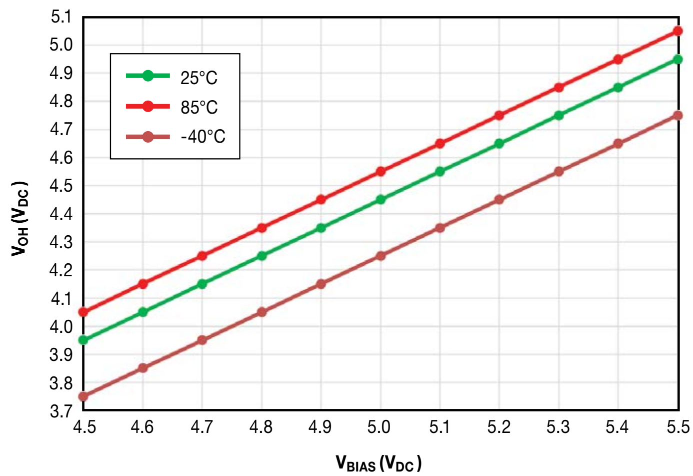


Figure 7. High-Side V_{OUT}-to-V_{BIAS} Relationship

Typical Application Information

The following figures detail the suggested applications for the FBS-GAM02P-C-PSE Module. For all applications, please refer to the implementation sections, following, for proper power supply bypassing and layout recommendations and criteria. In any of the following applications, the external HEMT transistors are EPC Space eGaN® power devices, appropriately rated for the voltage and current requirements of the application. If an inductive load is driven then an appropriately-rated Schottky rectifier/diode should be connected across the load to prevent destructive flyback/"kickback" voltages from destroying the external HEMT power switches. To keep power losses low, it is recommended to use a Schottky diode with the lowest possible V_f and C_j ratings for the "catch"/commutation diodes.

In all the following figures, only the pins that are considered or that require connection are identified.

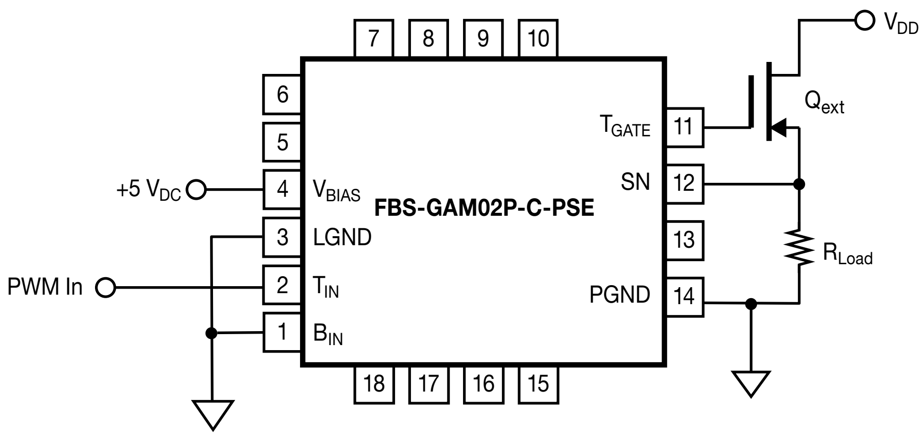


Figure 8. Single High-Side Power Switch Configuration

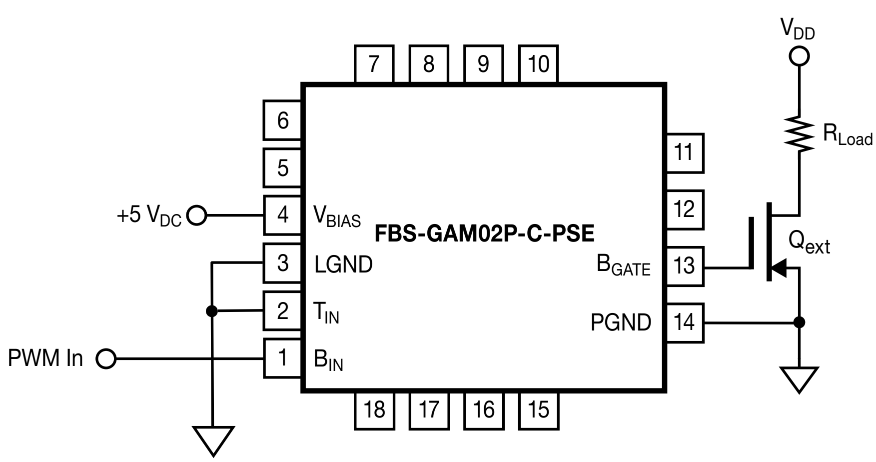


Figure 9. Single Low-Side Power Switch Configuration

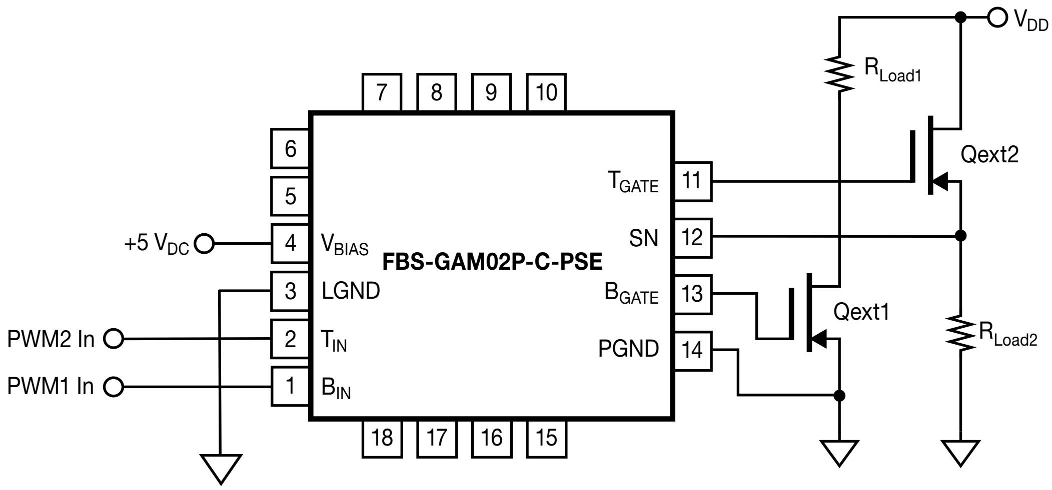


Figure 10. Independent High- and Low-Side Power Switches

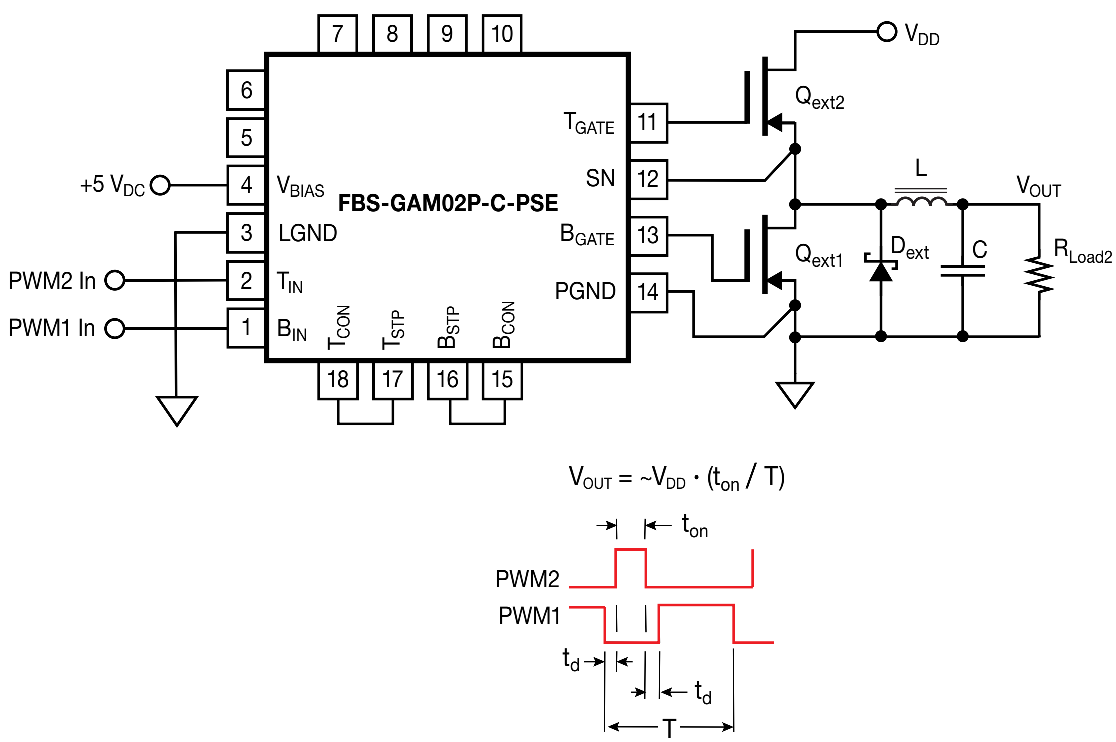


Figure 11. Half-Bridge Configuration: POL Converter Output Stage

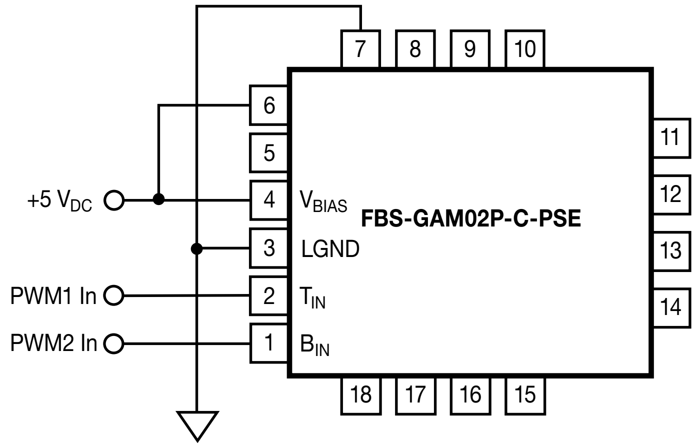


Figure 12. PG Protection Function Disabled

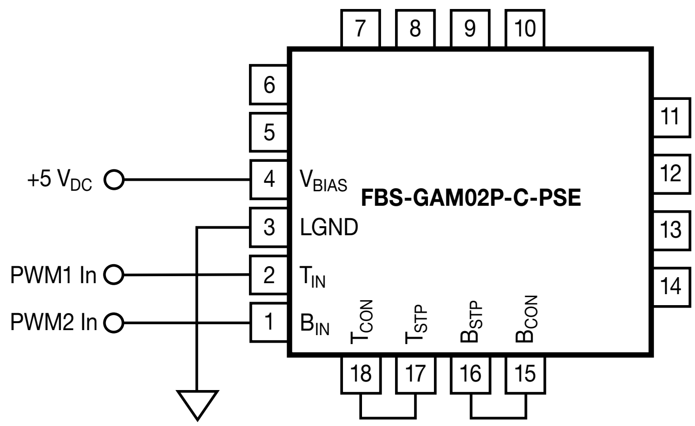


Figure 13. Shoot-Through Protection Function Enabled

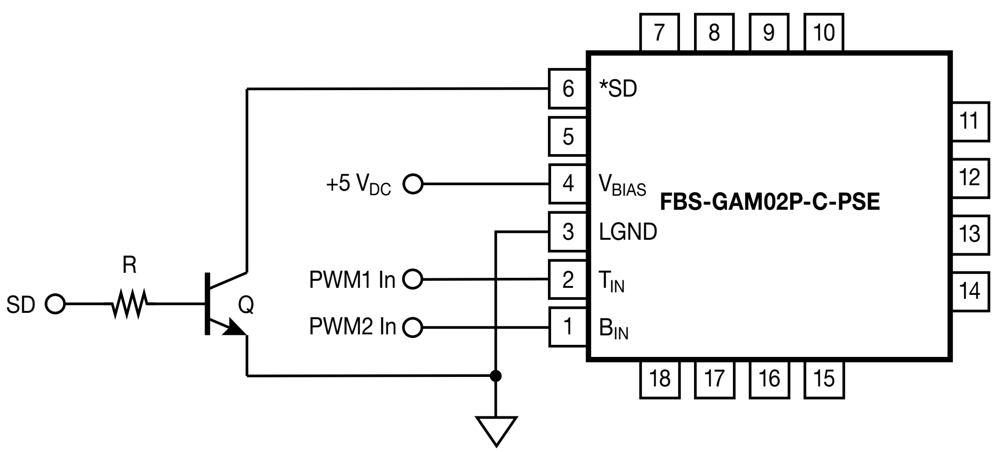


*Figure 14. *SD Input Function Enabled*

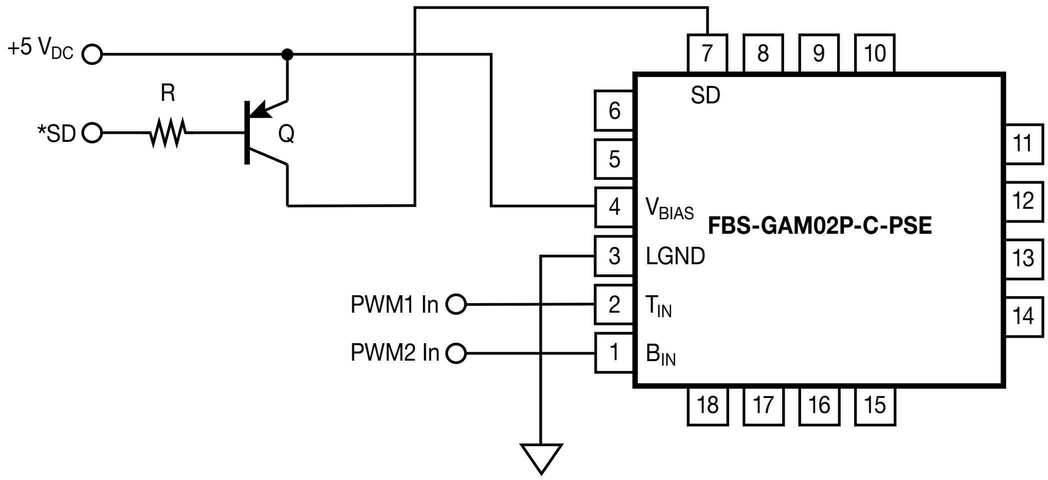


Figure 15. SD Input Function Enabled

Recommended External eGaN® HEMT Power Transistors

The recommended EPC Space eGaN® HEMT power transistors for various power supply voltages (V_{DD}) and load currents (I_D) for the Q_{ext}, Q_{ext1} and Q_{ext2} devices shown in Figures 8, 9, 10 and 11 are shown in Table I. Please note that the voltage and current values shown are NOT all de-rated, and appropriate de-rating guidelines should be used in space and mission-critical applications.

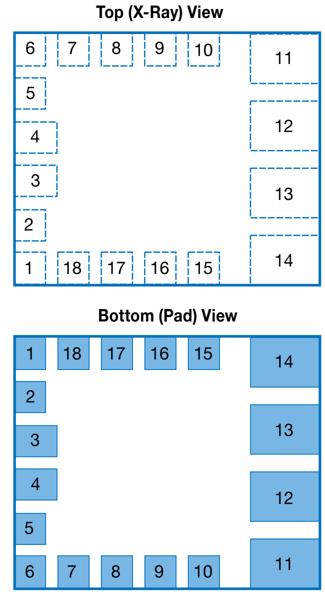
The FBS-GAM02P-C-PSE is capable of driving any of the devices shown in Table I without modification or additional circuitry. It should be noted that regardless of the voltage rating of the external power HEMT(s) utilized that the maximum voltage ratings of the FBS-GAM02P-C-PSE should be observed.

TABLE I. Recommended EPC Space eGaN® HEMT Power Transistors

V_{DD} (V_{DC})	I_O (A_{DC})	EPC Space P/N	$R_{DS(on)}$ (mΩ)	Package
40	8	FBG04N08AX	24	FSMD-A
40	30	FBG04N30BX	6	FSMD-B
100	5	FBG10N05AX	38	FSMD-A
100	30	FBG10N30BX	9	FSMD-B

Pin Descriptions

18 Pin Molded SMT Package with Pillar Pins



B_{IN} (Pin 1)

The B_{IN} pin is the logic input for low-side gate driver. When the B_{IN} input pin is logic low ("0"), the B_{GATE} pin (pin 13) is in the LOW (~PGND) state. When the IN1 pin is logic high ("1"), the B_{GATE} pin is in the HIGH (~V_{BIAS}) state.

T_{IN} (Pin 2)

The T_{IN} pin is the logic input for high-side gate driver. When the T_{IN} input pin is logic low ("0"), the T_{GATE} pin (pin 13) is in the LOW (~SN) state. When the IN1 pin is logic high ("1"), the T_{GATE} pin is in the HIGH (~TBST) state.

LGND (Pin 3)

Logic ground for the module. For proper operation of the FBS-GAM02P-C-PSE, the LGND pin (Pin 3) MUST be connected directly to the system logic ground return in the application circuit.

V_{BIAS} (Pin 4)

The V_{BIAS} pin is the raw input DC power input for the FBS-GAM02P-C-PSE module. It is recommended that a 1.0 microfarad ceramic capacitor and a 0.1 microfarad ceramic capacitor, each 25 V rating, be connected between V_{BIAS} (pin 4) and system power ground plane (the common tie point of PGND1 and PGND2) to obtain the specified switching performance.

PG (Power Good) (Pin 5)

The PG pin is an open drain logic-compatible output. For proper operation the PG pin must be pulled-up to V_{BIAS}, external to the module, with a 4.7 kΩ resistor.

The FBS-GAM02P-C-PSE incorporates a Power Good (PG) sensing circuit that disables both internal (low- and high-side) gate drivers when the +5 V gate drive bias potential (V_{BIAS}) falls below the under-voltage threshold, UVLO-, or rises above the V_{BIAS} over-voltage threshold level, OVLO+ (please refer to Figure 5 for the proper operational nomenclature and functionality versus the state of the V_{BIAS} power supply). During the time when the V_{BIAS} potential is outside of the pre-set threshold(s), the PG output (Pin 5) pin is logic low ("0"). Alternatively, when the V_{BIAS} potential is within the pre-set thresholds the PG pin is logic high ("1"). The logic condition of the PG pin may be sensed by an FPGA or Microcontroller/DSP in-order to determine when the power switches in the FBS-GAM02P-C-PSE may be driven with pulse-width modulated (PWM) input signal(s) at the B_{IN} and T_{IN} logic inputs. If either the under-voltage and over-voltage protection features are not required or desired, then these may be disabled by connecting the *SD (Pin 6) pin to V_{BIAS} (pin 4) and/or the SD pin (Pin 7) to LGND (pin 3), as shown in Figure 10.

*SD (Pin 6)

The *SD pin is a low-true disable input for the FBS-GAM02P-C-PSE module.

Both the low- and high-side gate drivers may be disabled (set to their OFF state) utilizing the *SD input, as shown in Figure 11. To disable the FBS-GAM02P-C-PSE module gate drive outputs, the *SD (Pin 6) input may be driven by an open drain or open collector that pulls this input to logic ground (LGND, pin 3). If the *SD shutdown function is not required, this pin should be left OPEN (no connection).

SD (Shutdown) (Pin 7)

The SD pin is a high-true disable input for the FBS-GAM02P-C-PSE module.

Both low- and high-side gate drivers may be disabled (set to their OFF state) utilizing the SD input, as shown in Figure 12. To disable the FBS-GAM02P-C-PSE module gate drive outputs, the SD (Pin 7) input may be driven by an open drain or open collector that pulls this input to VDRV (pin 1). If the SD shutdown function is not required, this pin should be left OPEN (no connection).

TOS (Pin 8)

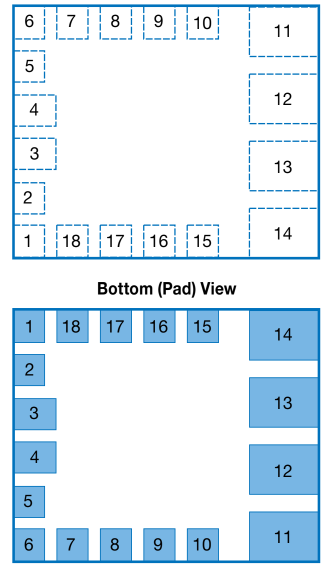
The TOS pin is the switching node (SN) sense pin. Pin 8 is internally connected to pin 12. The TOS pin acts as the return (i.e. "–" connection) for an external bootstrap capacitor or a floating DC power supply for the high-side driver.

Keep all connections to pin 8 as short as possible as the signals present at this pin are extremely high rate-of-voltage- change (dV/dt) signals. The TOS pin is internally-connected to SN (pin 12). If pin 8 is unused, it should be left OPEN ("no connection").

Pin Descriptions *(continued)*

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



N/C (Pin 9)

Pin 9 is not internally connected. This “no connection” pin is recommended to be connected to the system PGND (plane) as good engineering practice to avoid coupling unwanted noise into the internal circuitry of the FBS- GAM02P-C-PSE, either directly or via a 0 Ω jumper resistor.

TBST (Pin 10)

The TBST pin is the bootstrap bias supply for the high-side gate driver. The TBST pin acts as the supply (i.e. “+“ connection) for an external bootstrap capacitor or a floating DC power supply for the high-side driver. Keep all connections to pin 10 as short as possible as the signal present at this pin is an EXTREMELY HIGH rate-of-voltage-change (dV/dt) signal. If pin 10 is unused, it should be left OPEN (“no connection”).

T_{GATE} (Pin 11)

The T_{GATE} pin (pin 11) is the high peak current output for the internal high-side eGaN® HEMT driver associated with the T_{IN} logic input. This is an EXTREMELY HIGH dV/dt and dI/dt signal pin, and the connection to the external HEMT gate should be as short as possible to minimize radiated EMI and potential gate drive voltage ringing and damaging transients.

SN (Pin 12)

The SN pin (pin 12) is the switching node for the high-side gate driver and external power switch. The SN pin should be connected to the source sense (SS) pin of the external power eGaN® HEMT power switch. This connection provides a low inductance connection directly to the source of the external HEMT transistor. This is an EXTREMELY HIGH dV/dt and dI/dt signal pin, and the connection to the external HEMT source should be as short as possible to minimize radiated EMI and potential gate drive voltage ringing and damaging transients.

B_{GATE} (Pin 13)

The B_{GATE} pin (pin 13) is the high peak current output for the internal low-side eGaN® HEMT driver associated with the BIN logic input. This is an EXTREMELY HIGH dV/dt and dI/dt signal pin, and the connection to the external HEMT gate should be as short as possible to minimize radiated EMI and potential gate drive voltage ringing and damaging transients.

PGND1 (Pin 14)

The PGND pin (pin 14) is the ground return (source) connection for the internal power circuitry and for the low- side eGaN® HEMT gate driver associated with the BIN logic input. This pin should be connected directly to the source sense of the external power eGaN® HEMT power switch. To minimize unwanted transients and noise, the source of the HEMT associated with this pin should be tied directly to the power ground plane on the end-use PCB with the lowest possible impedance connection.

B_{CON} (Pin 15)

The B_{CON} pin is the logic input for the input shoot-through protection for low-side gate driver. The state of this pin follows the state of the B_{IN} logic input pin. If input shoot-through protection is desired, for example in the case of a half-bridge application (see Figure 9) where the low- and high-side gate drivers must not be turned on simultaneously, then B_{CON} (pin 15) should be externally connected to B_{STP} (pin 16). If no shoot-through protection is desired, then pin 15 should be left OPEN (no connection).

B_{STP} (Pin 16)

The B_{STP} pin is the open drain output for the input shoot-through protection for low-side gate driver. The state of this pin is the logical inverse of the T_{IN} logic input pin. If input shoot-through protection is desired, for example in the case of a half-bridge application (see Figure 9) where the low- and high-side gate drivers must not be turned on simultaneously, then B_{STP} (pin 16) should be externally connected to B_{CON} (pin 15). If no shoot-through protection is desired, then pin 16 should be left OPEN (no connection).

T_{STP} (Pin 17)

The T_{STP} pin is the open drain output for the input shoot-through protection for high-side gate driver. The state of this pin is the logical inverse of the B_{IN} logic input pin. If input shoot-through protection is desired, for example in the case of a half-bridge application (see Figure 9) where the low- and high-side gate drivers must not be turned on simultaneously, then T_{STP} (pin 17) should be externally connected to T_{CON} (pin 18). If no shoot-through protection is desired, then pin 17 should be left OPEN (no connection).

T_{CON} (Pin 18)

The T_{CON} pin is the logic input for the input shoot-through protection for high-side gate driver. The state of this pin follows the state of the T_{IN} logic input pin. If input shoot-through protection is desired, for example in the case of a half-bridge application (see Figure 9) where the low- and high-side gate drivers must not be turned on simultaneously, then T_{CON} (pin 18) should be externally connected to T_{STP} (pin 17). If no shoot-through protection is desired, then pin 18 should be left OPEN (no connection).

Recommended V_{BIAS}-to-PGND Power Supply Bypassing

The power supply pins and return pin of the FBS-GAM02P-C-PSE require proper high frequency bypassing to one-another in order to prevent harmful switching noise-related spikes from degrading or damaging the internal circuitry in the FBS-GAM02P-C-PSE module. It is recommended that a 1.0 microfarad ceramic capacitor and a 0.1 microfarad ceramic capacitor, each 25 V rating, be connected between V_{BIAS} (pin 4) and PGND (pin 14).

Suggested FBS-GAM02P-C-PSE Schematic Symbol

The suggested schematic symbol for the FBS-GAM02P-C-PSE is shown in Figure 6. This symbol groups the I/O pins of the FBS-GAM02P-C-PSE into groups of similar functionality.

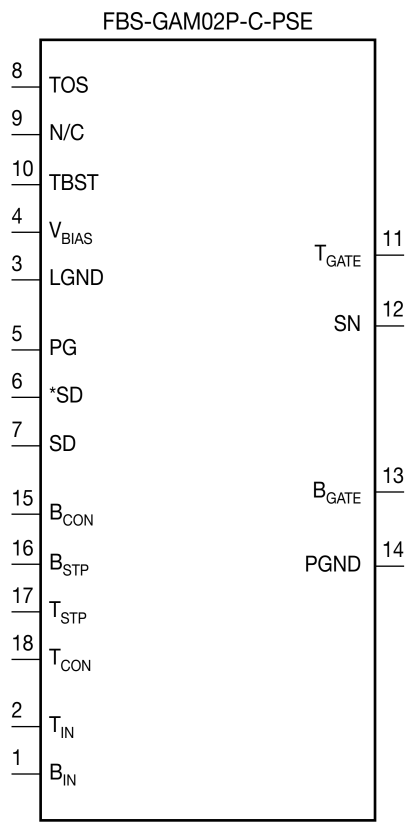
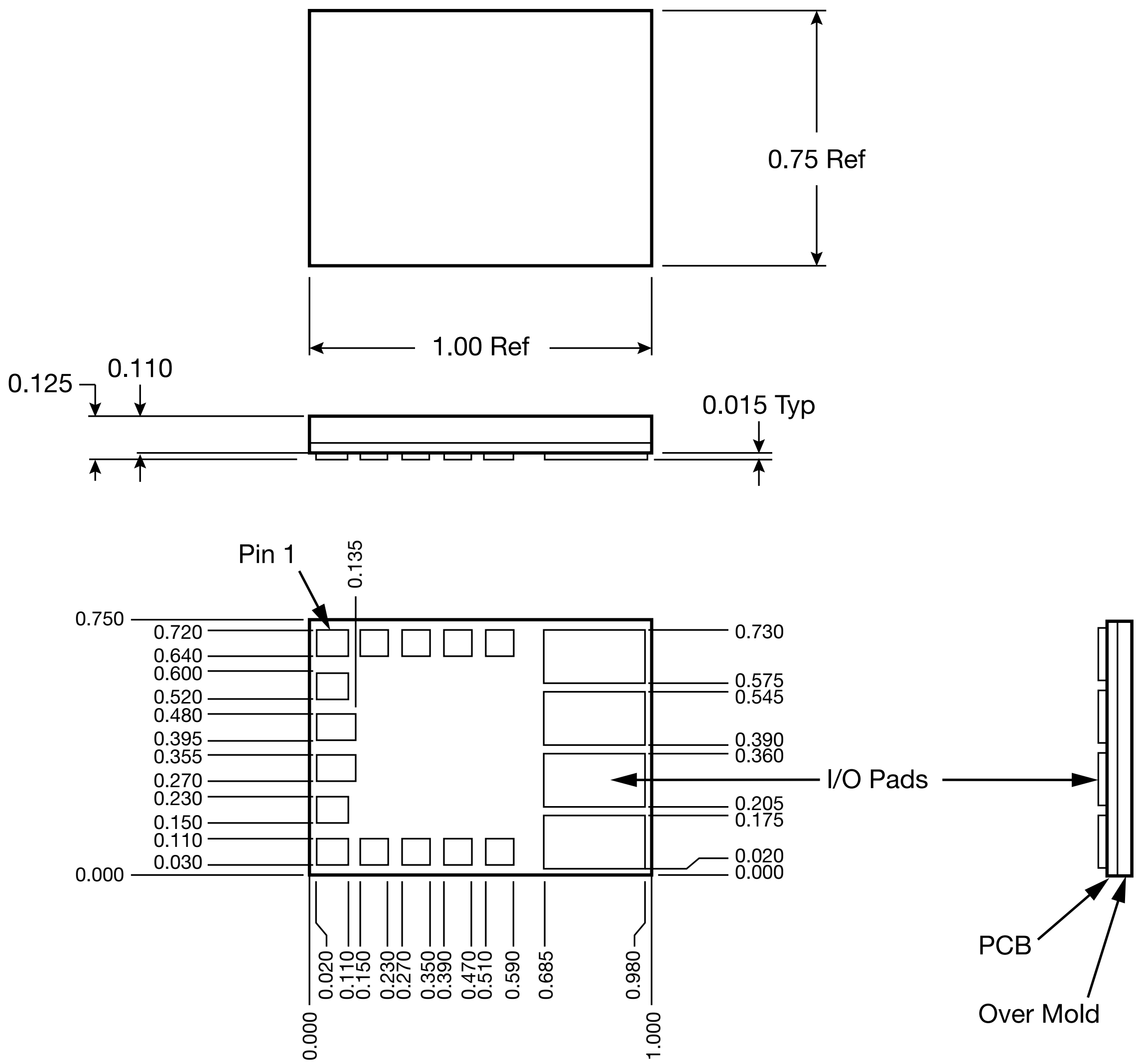


Figure 16. Suggested FBS-GAM02P-C-PSE Schematic Symbol

Package Outline and Dimensions



Note: All dimensions are in inches
ALL tolerances +/- 0.010

Figure 17. FBS-GAM02P-C-PSE Package Outline and Dimensions

Recommended PCB Solder Pad Configuration

The novel I/O "pillar" pads fabricated onto the bottom surface of the FBS-GAM02P-C-PSE module are designed to provide optimal electrical, thermal and mechanical properties for the end-use system designer. To achieve the full benefit of these properties, it is important that the FBS-GAM02P-C-PSE module be soldered to the PCB motherboard using SN63 (or equivalent) solder. The recommended pad dimensions and locations are shown in Figure 18. All dimensions are shown in inches.

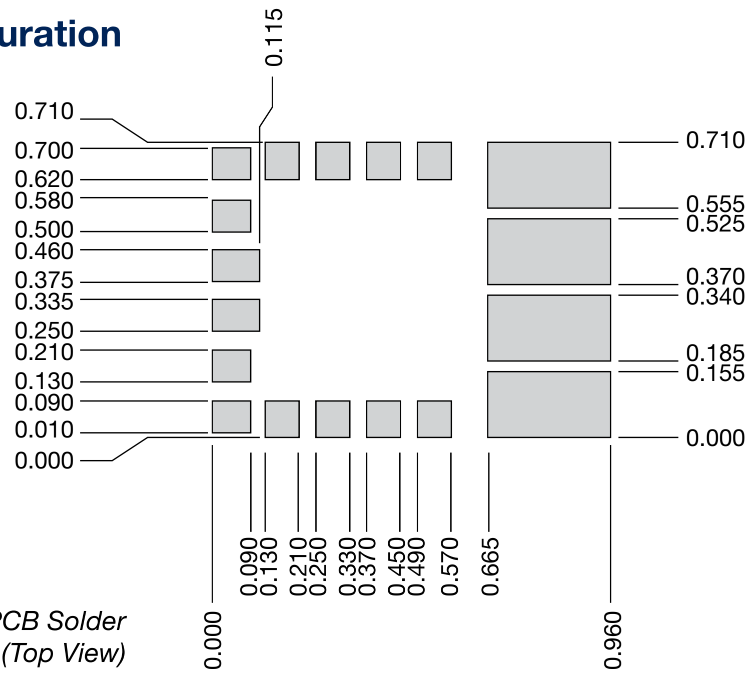


Figure 18. Recommended PCB Solder Pad Configuration (Top View)

Sn63/Pb37 No Clean Solder Paste Typical Example Profile

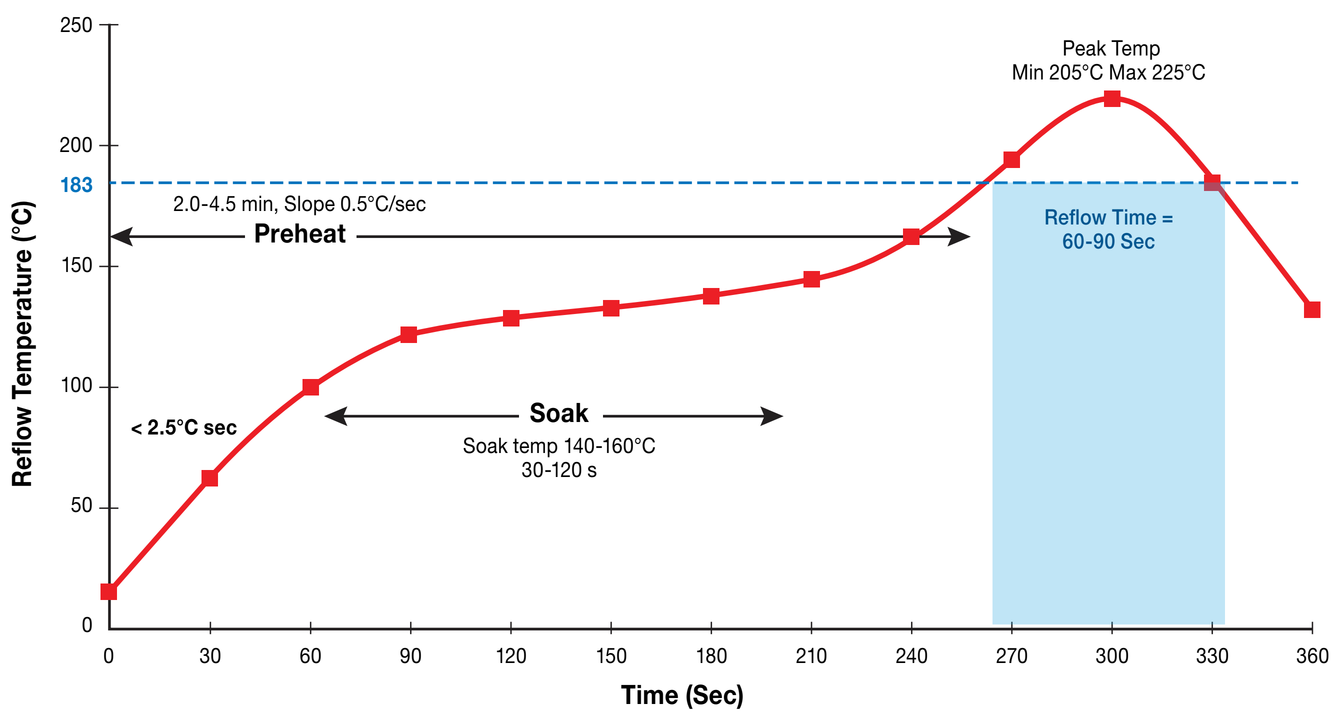


Figure 19. Typical GAM02P-PSE Solder Reflow Profile

Preheat Zone – The preheat zone, is also referred to as the ramp zone, and is used to elevate the temperature of the PCB to the desired soak temperature. In the preheat zone the temperature of the PCB is constantly rising, at a rate that should not exceed 2.5°C/sec. The oven's preheat zone should normally occupy 25-33% of the total heated tunnel length.

The Soak Zone – normally occupies 33-50% of the total heated tunnel length exposes the PCB to a relatively steady temperature that will allow the components of different mass to be uniform in temperature. The soak zone also allows the flux to concentrate and the volatiles to escape from the paste.

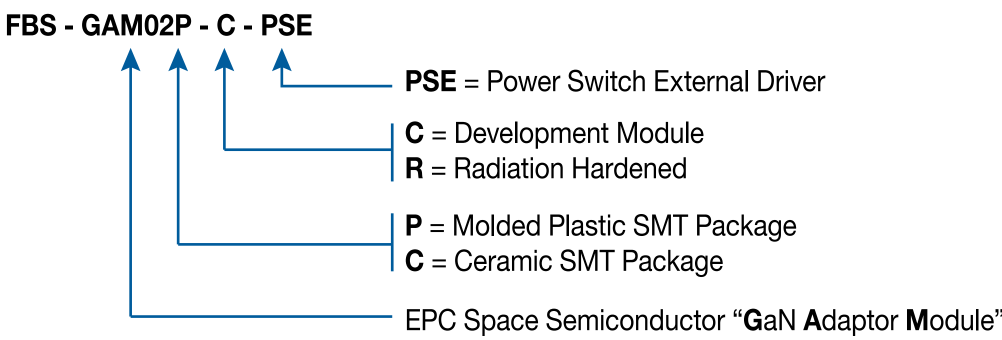
The Reflow Zone – or spike zone is to elevate the temperature of the PCB assembly from the activation temperature to the recommended peak temperature. The activation temperature is always somewhat below the melting point of the alloy, while the peak temperature is always above the melting point.

Reflow – Best results achieved when reflowed in a forced air convection oven with a minimum of 8 zones (top & bottom), however reflow is possible with a four-zone oven (top & bottom) with the recommended profile for a forced air convection reflow process. The melting temperature of the solder, the heat resistance of the components, and the characteristics of the PCB (i.e. density, thickness, etc.) determine the actual reflow profile.

Note: FBS-GAM02P-C-PSE solder attachment has a maximum peak dwell temperature of 230°C limit, exceeding the maximum peak temperature can cause damage the unit.

Reflow Process Disclaimer
The profile is as stated “Example”. The-end user can optimize reflow profiling based against the actual solder paste and reflow oven used. EPC Space assumes no liability in conjunction with the use of this profile information.

EPC Space Part Number Information



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Revisions

Datasheet Revision	Product Status
REV -	Proposal/development
M-702-010-Q1	Characterization and Qualification
	Production Released

Information subject to change without notice.
Revised February, 2023