

MOSFET – Dual, N-Channel, Asymmetric, Power Clip, POWER trench[®], 30 V

FDPC8013S

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

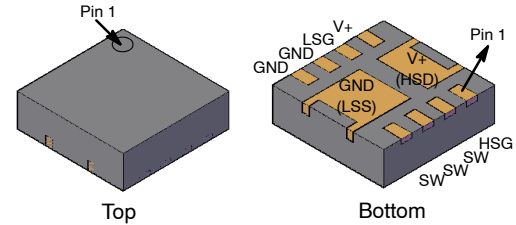
- Max $R_{DS(on)}$ = 9.6 mΩ at V_{GS} = 4.5 V, I_D = 10 A

Q2: N-Channel

- Max $R_{DS(on)}$ = 2.7 mΩ at V_{GS} = 4.5 V, I_D = 22 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- RoHS Compliant

Applications

- Computing
- Communications
- General Purpose Point of Load



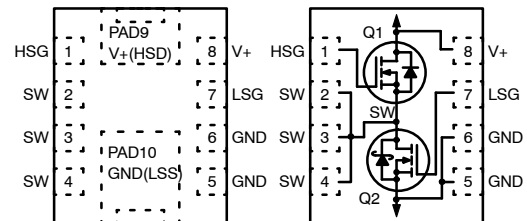
PQFN8 3.3 × 3.3, 0.65P
CASE 483AZ

MARKING DIAGRAM

&Z&3&K
13CF
15CF

&Z = Assembly Plant Code
&3 = 3-Digit Date Code
&K = 2-Digits Lot Run Traceability Code
13CF15CF = Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDPC8013S	PQFN8	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://www.onsemi.com/BRD8011/D).

FDPC8013S

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit
V _{DS}	Drain to Source Voltage		30	30	V
V _{GS}	Gate to Source Voltage		±20	±20	V
I _D	Drain Current	– Continuous (Package limited) T _C = 25°C	20	55	A
		– Continuous T _A = 25°C	13 (Note 1a)	26 (Note 1b)	
		– Pulsed	40	100	
E _{AS}	Single Pulse Avalanche Energy (Note 3)		21	97	mJ
P _D	Power Dissipation for Single Operation	T _A = 25°C	1.6 (Note 1a)	2.0 (Note 1b)	W
		T _A = 25°C	0.8 (Note 1c)	0.9 (Note 1d)	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Value	Unit
R _{θJA}	Thermal Resistance, Junction to Ambient	77 (Note 1a)	63 (Note 1b)	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient	151 (Note 1c)	135 (Note 1d)	
R _{θJC}	Thermal Resistance, Junction to Case	5.0	3.5	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = 1 mA, V _{GS} = 0 V	Q1 Q2	30 30	– –	– –	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2	– –	16 20	– –	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V V _{DS} = 24 V, V _{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V V _{GS} = 20 V, V _{DS} = 0 V	Q1 Q2	– –	– –	100 100	nA nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA V _{GS} = V _{DS} , I _D = 1 mA	Q1 Q2	1.2 1.2	1.5 1.7	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2	– –	–5 –6	– –	mV/°C
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10 V, I _D = 13 A V _{GS} = 4.5 V, I _D = 10 A V _{GS} = 10 V, I _D = 13 A, T _J = 125°C	Q1	– – –	4.6 6.7 6.6	6.4 9.6 9.2	mΩ
		V _{GS} = 10 V, I _D = 26 A V _{GS} = 4.5 V, I _D = 22 A V _{GS} = 10 V, I _D = 26 A, T _J = 125°C	Q2	– – –	1.4 2.0 1.9	1.9 2.7 2.6	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 13 A	Q1	–	53	–	S
		V _{DS} = 5 V, I _D = 26 A	Q2	–	168	–	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	Q1: V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz Q2: V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	827 2785	– –	pF
C _{oss}	Output Capacitance		Q1 Q2	– –	333 997	– –	pF
C _{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	44 128	– –	pF
R _g	Gate Resistance		Q1	–	0.5	–	Ω
			Q2	–	0.5	–	

FDPC8013S

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

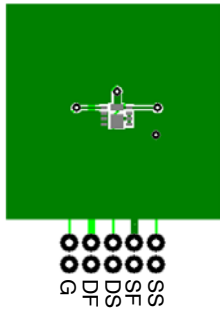
Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 15\text{ V}$, $I_D = 13\text{ A}$, $R_{GEN} = 6\ \Omega$ Q2: $V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$, $R_{GEN} = 6\ \Omega$	Q1	–	6	–	ns
t_r	Rise Time		Q2	–	11	–	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1	–	2	–	ns
t_f	Fall Time		Q2	–	5	–	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	Q1	–	13	–	nC
		$V_{GS} = 0\text{ V to }4.5\text{ V}$	Q2	–	44	–	nC
Q_{gs}	Gate to Source Gate Charge	Q1 $V_{DD} = 15\text{ V}$, $I_D = 13\text{ A}$ Q2 $V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$	Q1	–	6	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		Q2	–	21	–	nC
Q_{gs}	Gate to Source Gate Charge	Q1 $V_{DD} = 15\text{ V}$, $I_D = 13\text{ A}$ Q2 $V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$	Q1	–	2.2	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		Q2	–	7.2	–	nC
Q_{gs}	Gate to Source Gate Charge	Q1 $V_{DD} = 15\text{ V}$, $I_D = 13\text{ A}$ Q2 $V_{DD} = 15\text{ V}$, $I_D = 26\text{ A}$	Q1	–	1.9	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		Q2	–	6.6	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

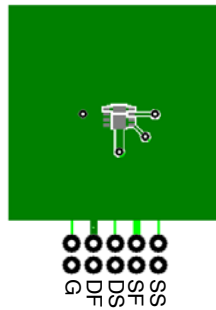
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 13\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}$, $I_S = 26\text{ A}$ (Note 2)	Q1	–	0.80	1.2	V
t_{rr}	Reverse Recovery Time	Q1: $I_F = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q1	–	22	–	ns
Q_{rr}	Reverse Recovery Charge	Q2: $I_F = 26\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$	Q2	–	29	–	ns
			Q1	–	7	–	nC
			Q2	–	30	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $77^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $63^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



c. $151^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper



d. $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- Q1: E_{AS} of 21 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 1.2\text{ mH}$, $I_{AS} = 6\text{ A}$, $V_{DD} = 23\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 14.5\text{ A}$.
Q2: E_{AS} of 97 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 0.6\text{ mH}$, $I_{AS} = 18\text{ A}$, $V_{DD} = 23\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 32.9\text{ A}$.
- As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

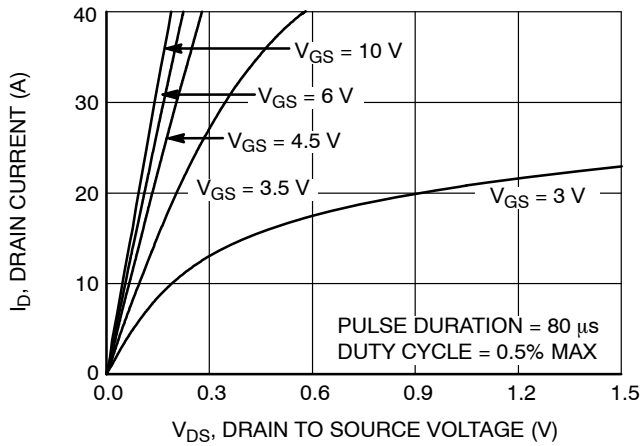


Figure 1. On-Region Characteristics

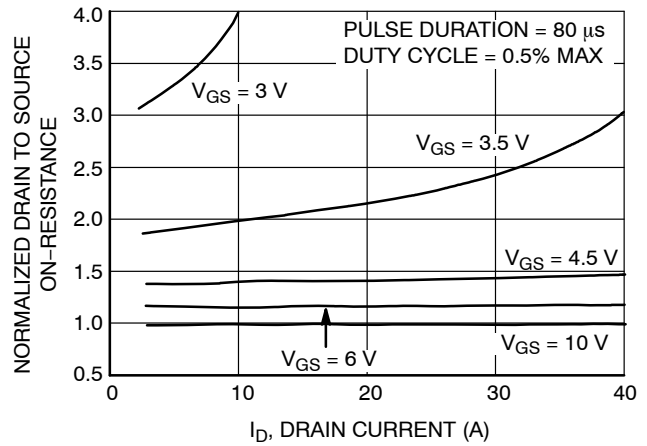


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

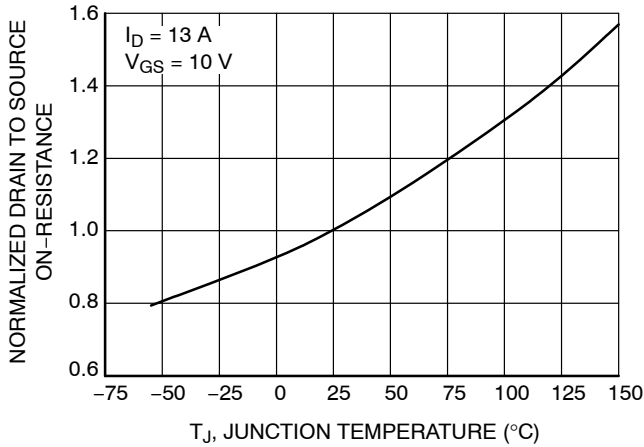


Figure 3. Normalized On-Resistance vs. Junction Temperature

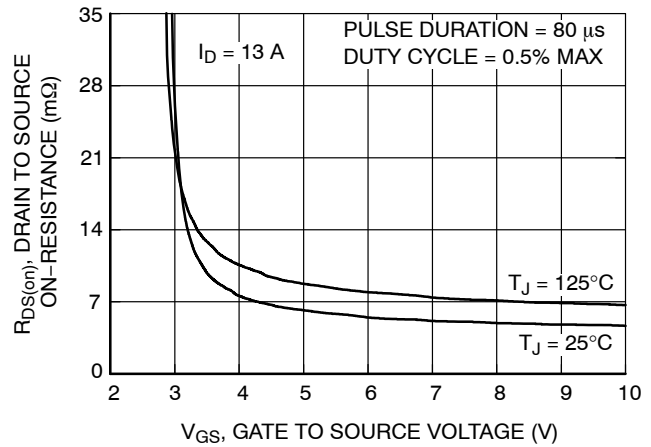


Figure 4. On-Resistance vs. Gate to Source Voltage

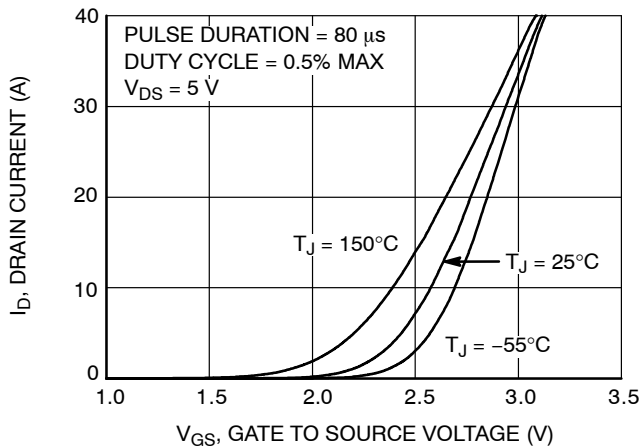


Figure 5. Transfer Characteristics

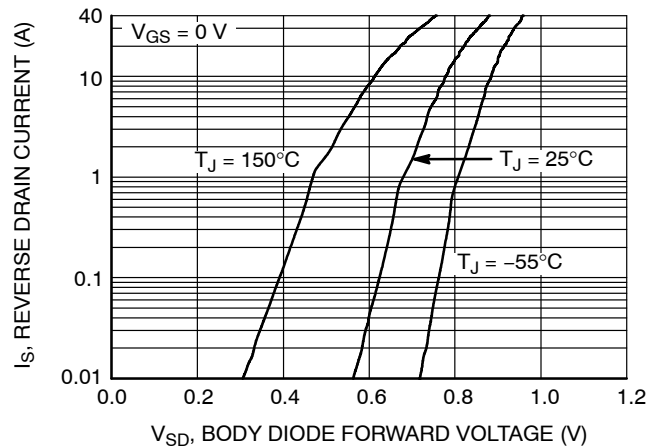


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

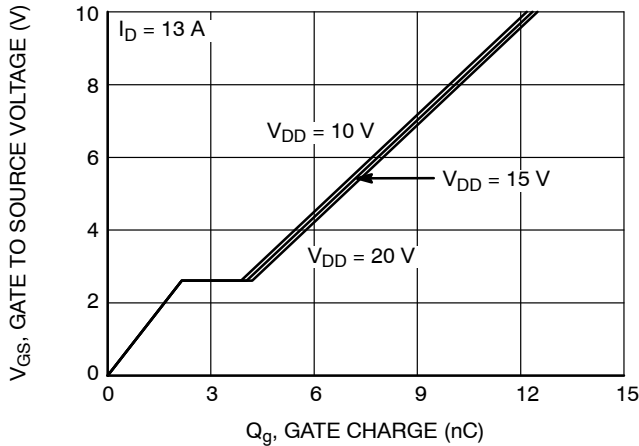


Figure 7. Gate Charge Characteristics

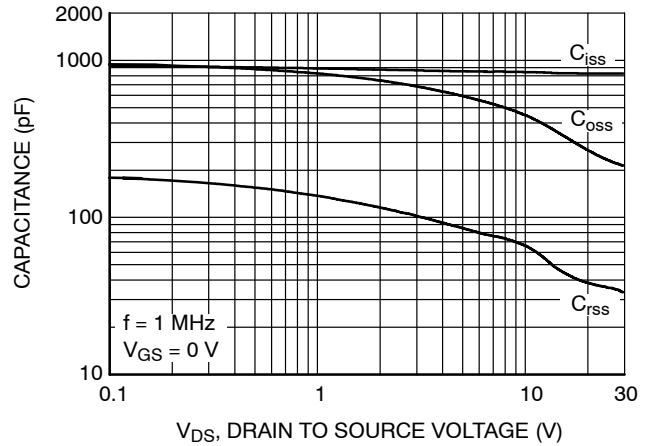


Figure 8. Capacitance vs. Drain to Source Voltage

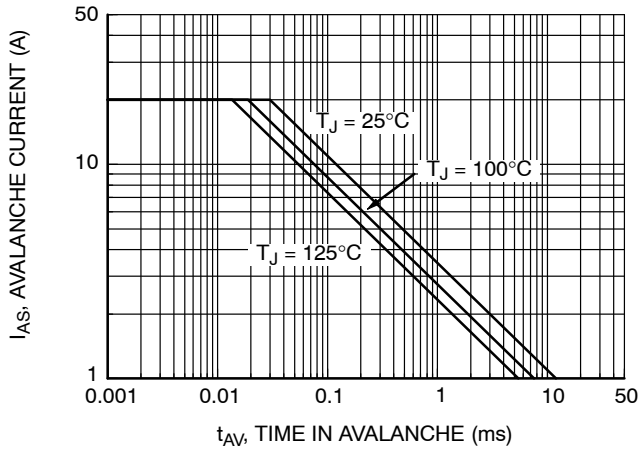


Figure 9. Unclamped Inductive Switching Capability

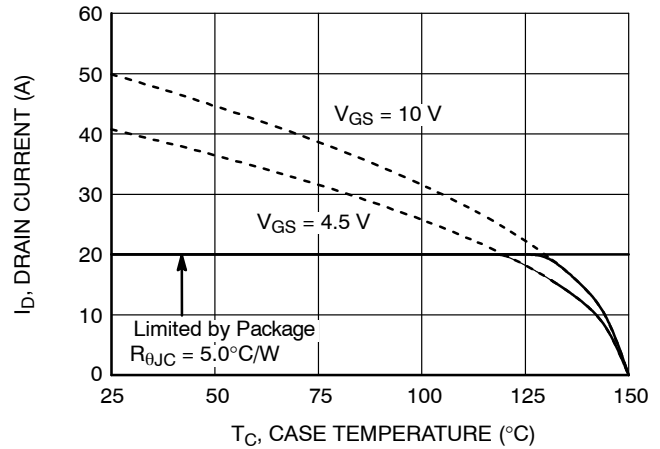


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

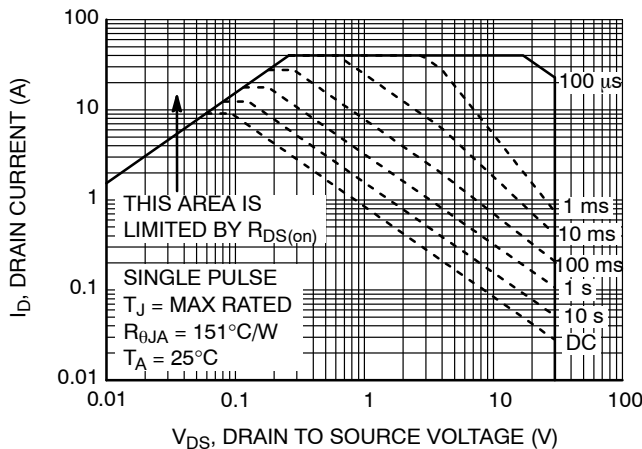


Figure 11. Forward Bias Safe Operating Area

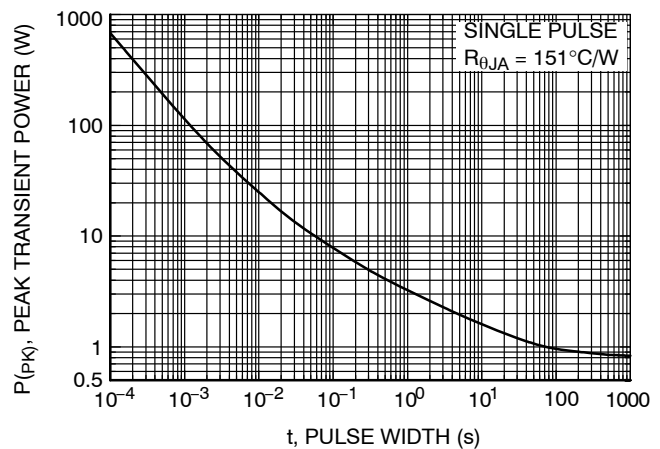


Figure 12. Single Pulse Maximum Power Dissipation

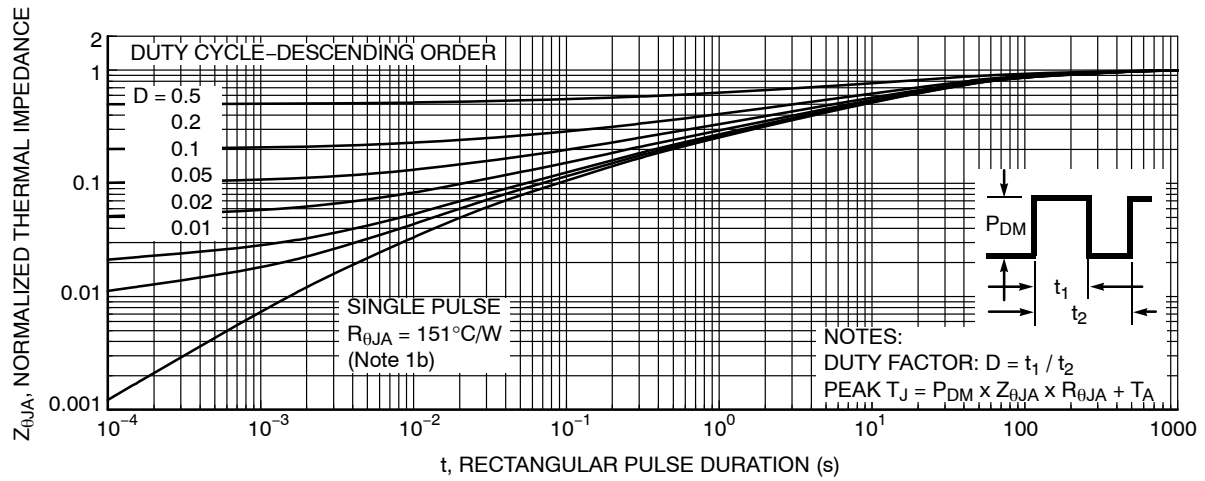
TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Figure 13. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

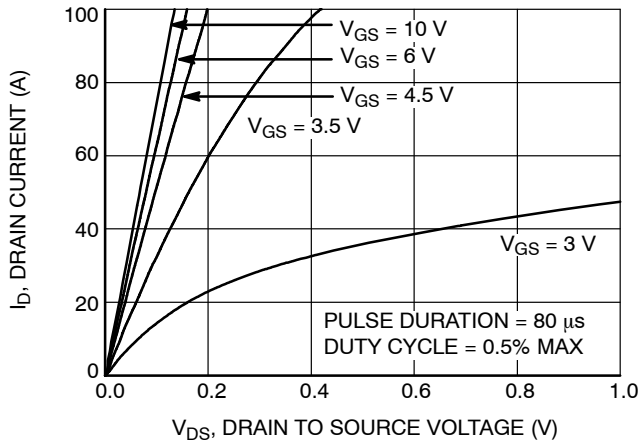


Figure 14. On-Region Characteristics

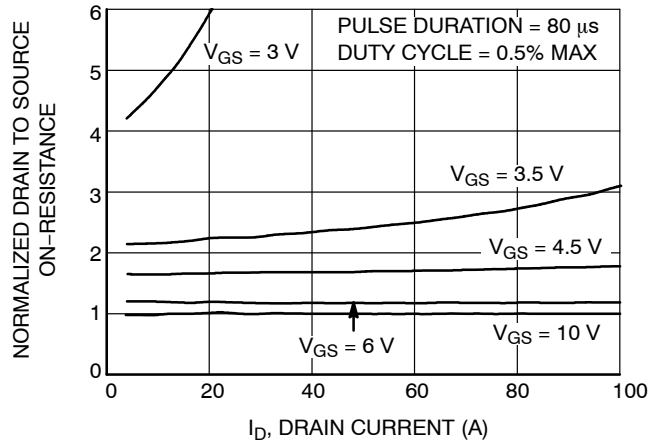


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

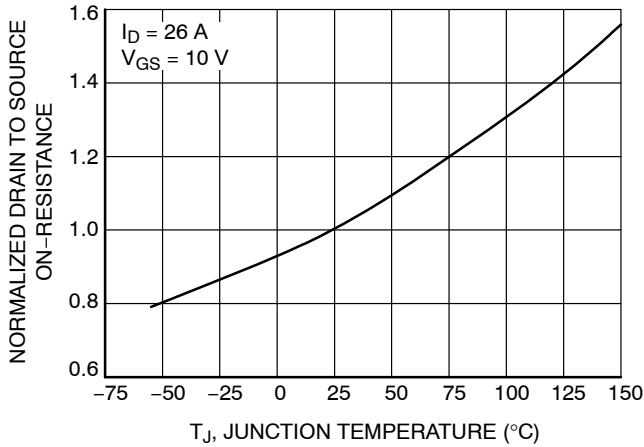


Figure 16. Normalized On-Resistance vs. Junction Temperature

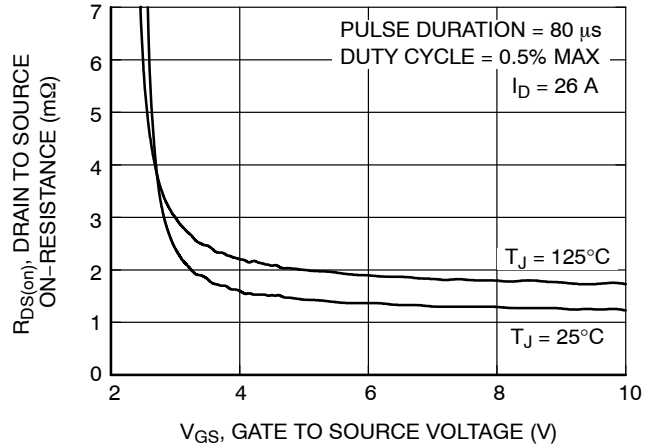


Figure 17. On-Resistance vs. Gate to Source Voltage

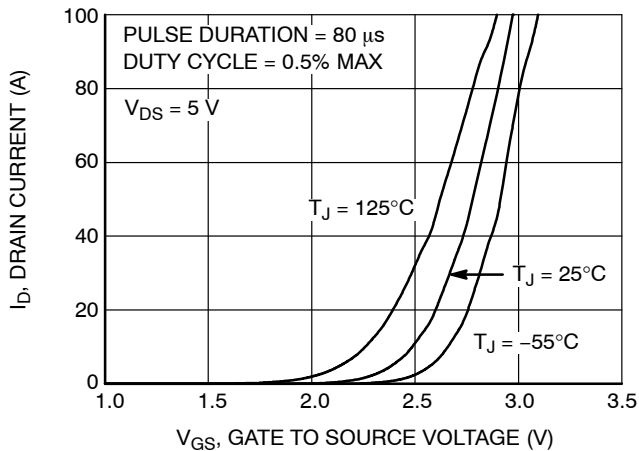


Figure 18. Transfer Characteristics

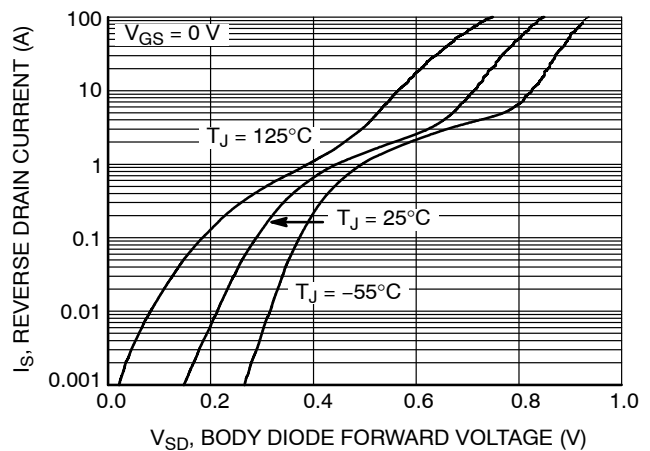


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

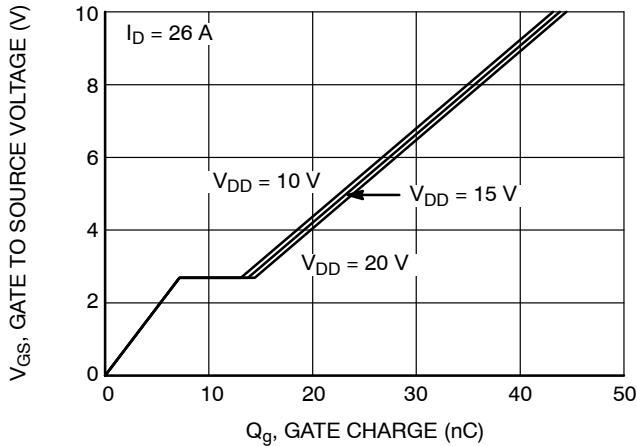


Figure 20. Gate Charge Characteristics

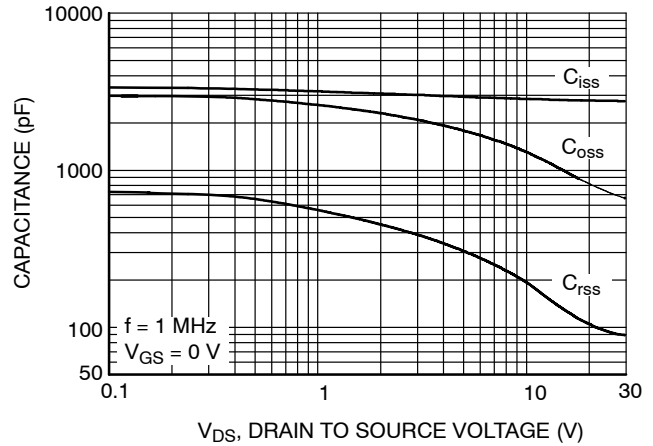


Figure 21. Capacitance vs. Drain to Source Voltage

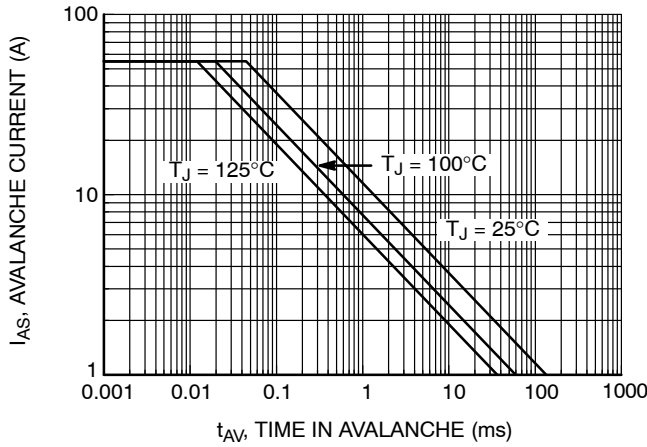


Figure 22. Unclamped Inductive Switching Capability

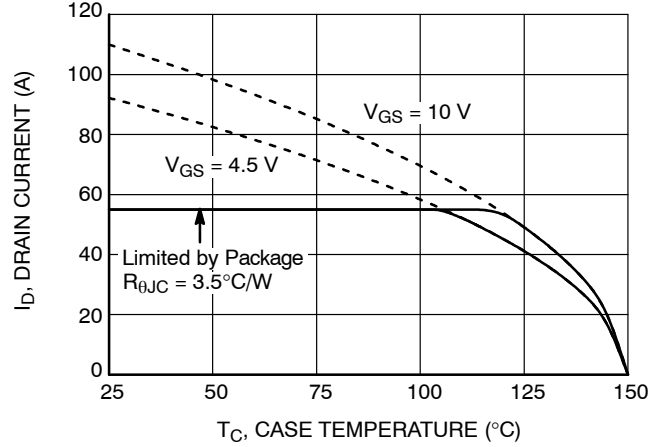


Figure 23. Maximum Continuous Drain Current vs. Ambient Temperature

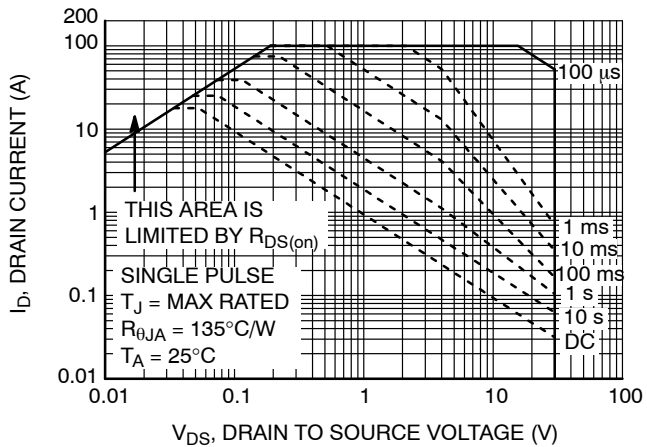


Figure 24. Forward Bias Safe Operating Area

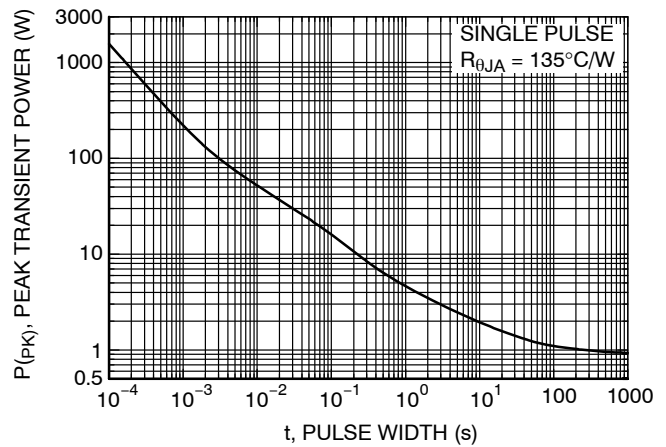


Figure 25. Single Pulse Maximum Power Dissipation

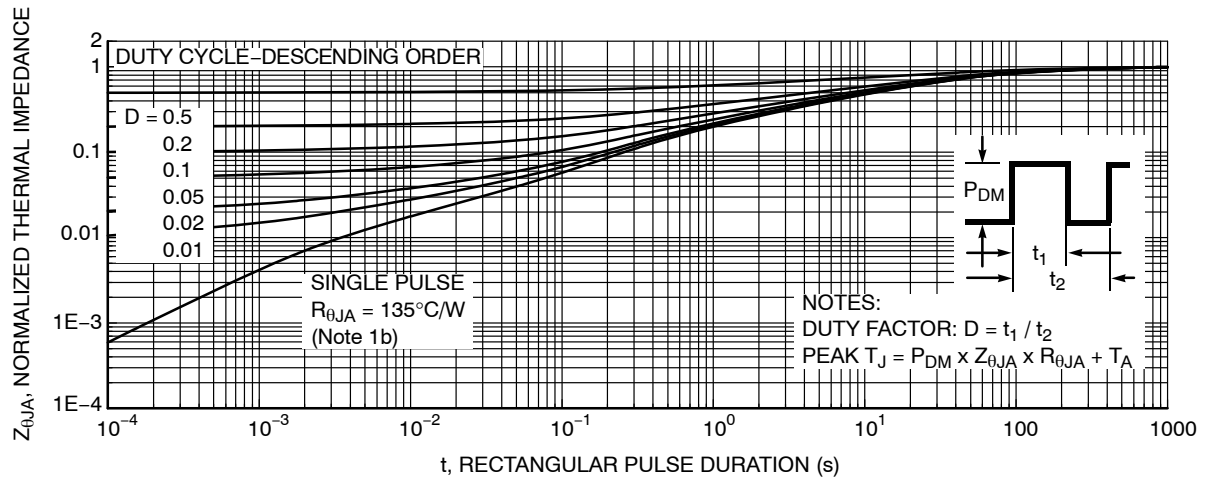
TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Figure 26. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8013S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

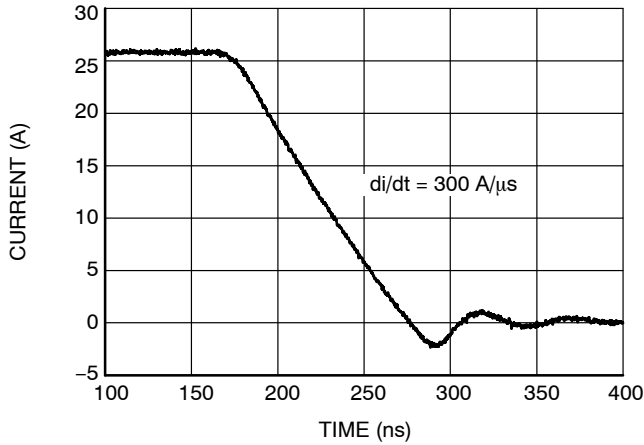


Figure 27. FDPC8013S SyncFET Body Diode Reverse Recovery Characteristics

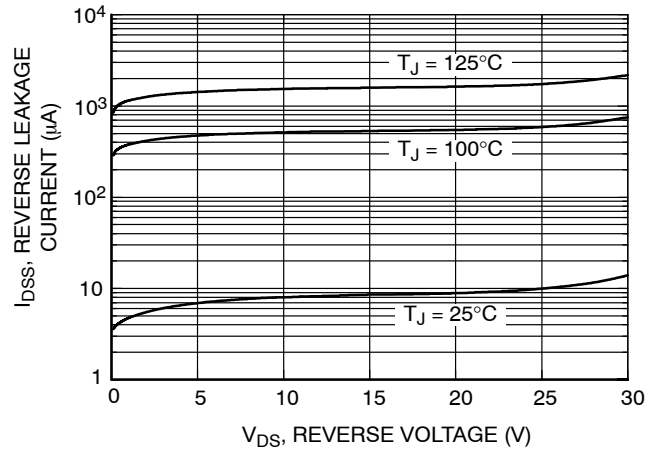
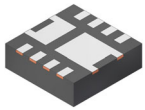


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

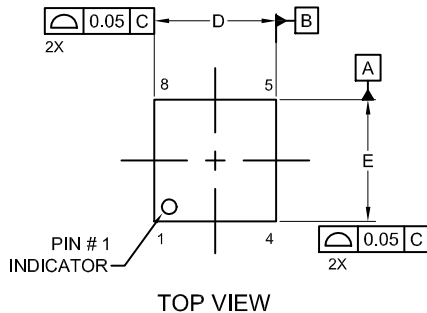
POWERTRENCH is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

SyncFET is a trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

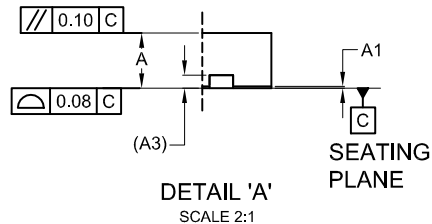


PQFN8 3.3X3.3, 0.65P
CASE 483AZ
ISSUE B

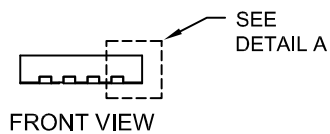
DATE 14 FEB 2022



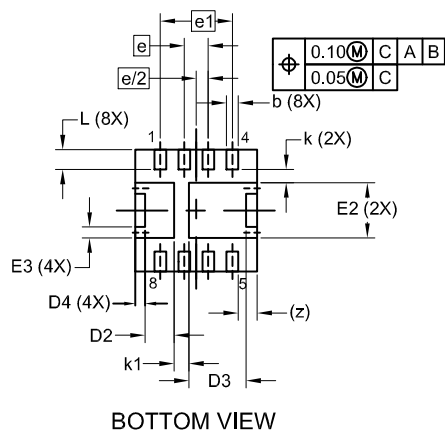
TOP VIEW



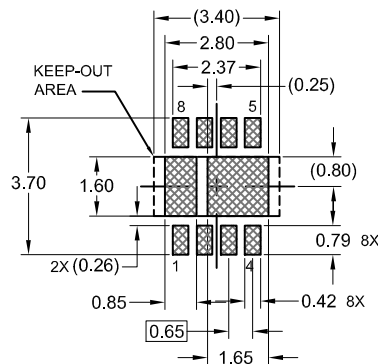
DETAIL 'A'
SCALE 2:1



FRONT VIEW



BOTTOM VIEW

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	0.69	0.79	0.89
D3	1.45	1.55	1.65
D4	0.16	0.26	0.36
E	3.20	3.30	3.40
E2	1.40	1.50	1.60
E3	0.30 REF		
e	0.65 BSC		
e1	1.95 BSC		
e/2	0.325 BSC		
k	0.36 REF		
k1	0.40 REF		
L	0.44	0.54	0.64
z	0.52 REF		

DOCUMENT NUMBER:	98AON13675G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PQFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

onsemi and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales