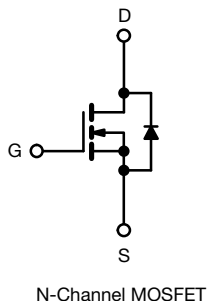
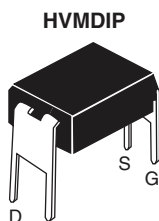


Power MOSFET



FEATURES

- For automatic insertion
- Compact, end stackable
- Fast switching
- Ease of paralleling
- Excellent temperature stability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



DESCRIPTION

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness. HVMDIPs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HVMDIP 4 pin, dual-in-line package brings the advantages of HVMDIPs to high volume applications where automatic PC board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment, and consumer products. Their compatibility with automatic insertion equipment, low-profile and end stackable features represent the state-of-the-art in power device packaging.

PRODUCT SUMMARY

V_{DS} (V)	50	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.10
Q_g (Max.) (nC)	24	
Q_{gs} (nC)	7.1	
Q_{gd} (nC)	7.1	
Configuration	Single	

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD020PbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage ^a	V_{DS}	50	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	19	W/ $^\circ\text{C}$
Linear derating factor		0.0080	
Inductive current, clamped	I_{LM}	19	A
Unclamped inductive current (avalanche current) ^c	I_L	2.2	
Maximum power dissipation	P_D	1.0	W
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering recommendations (peak temperature)	For 10 s	300 ^d	

Notes

- $T_J = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 100\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_C = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		50	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = max. rating, V _{GS} = 0 V		-	-	250	μA
		V _{DS} = max. rating x 0.8, V _{GS} = 0 V, T _C = 125		-	-	1000	
On-State Drain Current ^b	I _{D(on)}	V _{GS} = 10 V	V _{DS} > I _{D(on)} x R _{DS(on)} max.	2.4	-	-	A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.4 A	-	0.080	0.10	Ω
Forward Transconductance ^b	g _{fs}	V _{DS} = 20 V, I _D = 7.5 A		4.9	7.3	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz		-	400	-	pF
Output Capacitance	C _{oss}			-	260	-	
Reverse Transfer Capacitance	C _{rss}			-	44	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 15 A, V _{DS} = max. rating x 0.8	-	16	24	nC
Gate-Source Charge	Q _{gs}			-	4.7	7.1	
Gate-Drain Charge	Q _{gd}			-	4.7	7.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, I _D = 15 A, R _g = 18 Ω, R _D = 1.7 Ω		-	8.7	13	ns
Rise Time	t _r			-	55	83	
Turn-Off Delay Time	t _{d(off)}			-	16	24	
Fall Time	t _f			-	26	39	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.4	A
Pulsed Diode Forward Current ^c	I _{SM}			-	-	19	
Body Diode Voltage ^a	V _{SD}	T _C = 25 °C, I _S = 2.4 A, V _{GS} = 0 V		-	-	1.4	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 15 A, dI/dt = 100 A/μs		57	130	310	ns
Body Diode Reverse Recovery Charge	Q _{rr}			0.17	0.34	0.85	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 100\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$

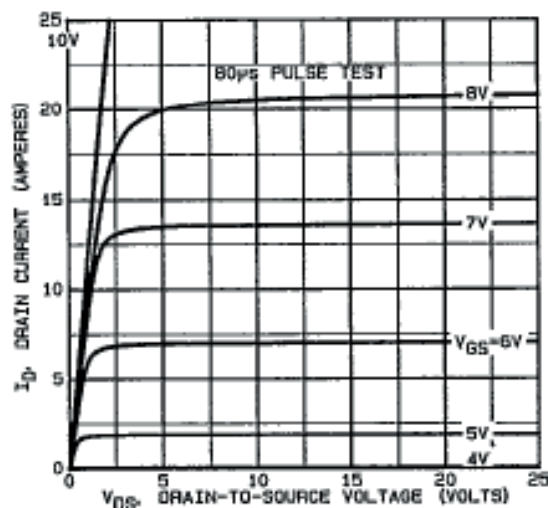
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Fig. 1 - Typical Output Characteristics

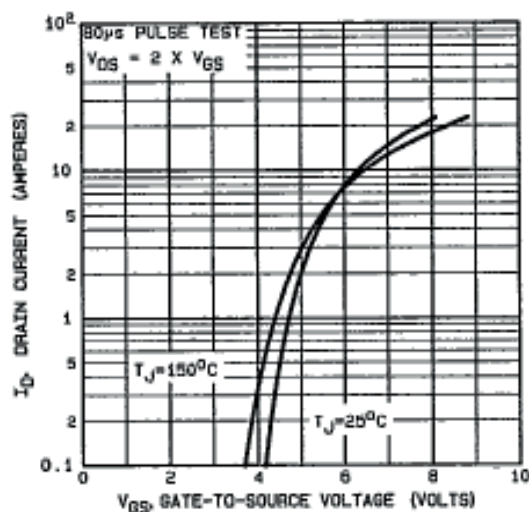


Fig. 3 - Typical Transfer Characteristics

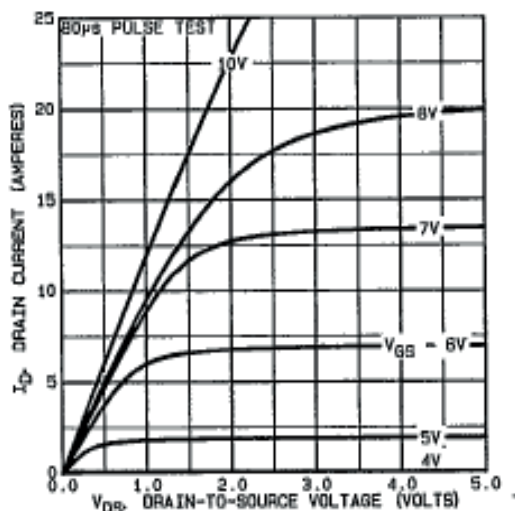


Fig. 2 - Typical Output Characteristics

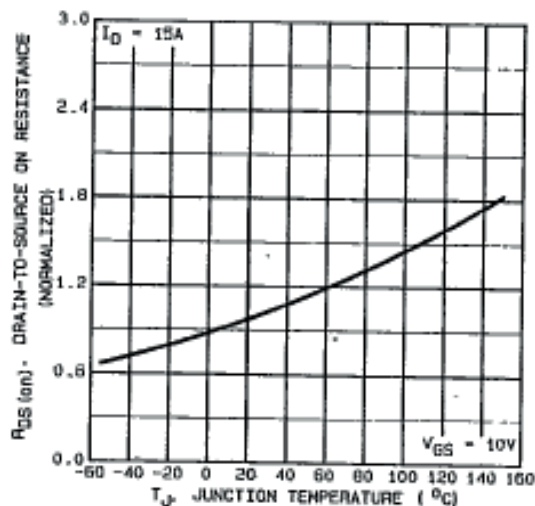


Fig. 4 - Normalized On-Resistance vs. Temperature

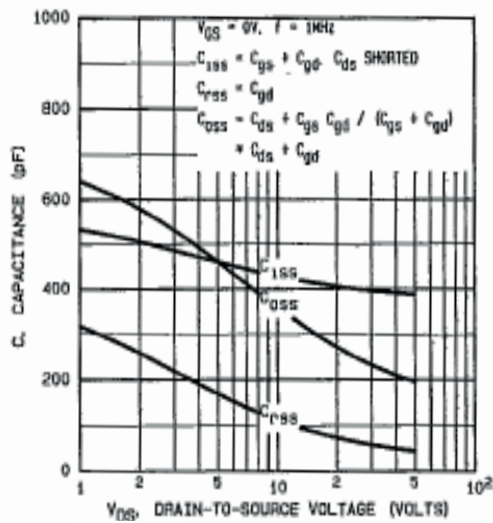


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

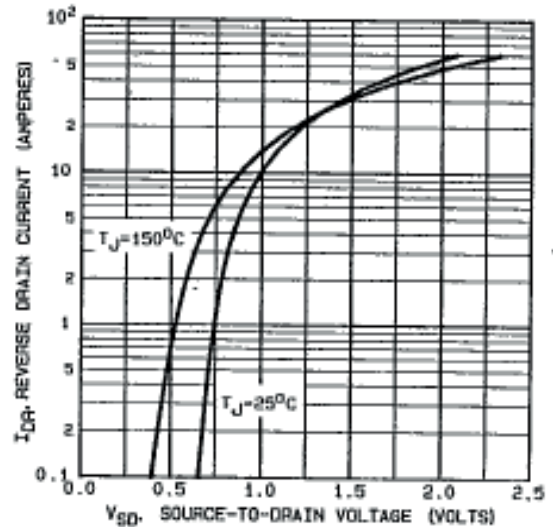


Fig. 7 - Typical Source-Drain Diode Forward Voltage

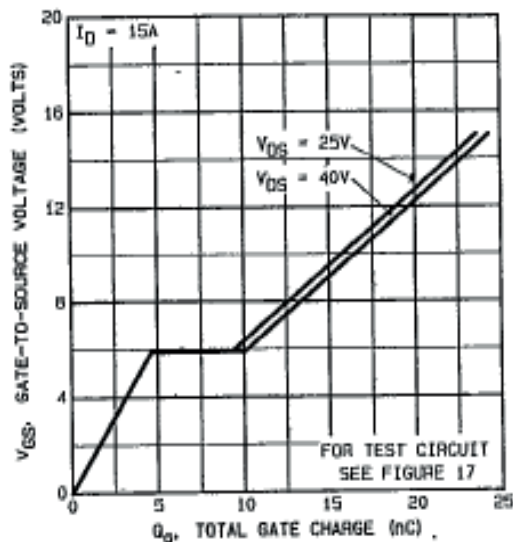


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

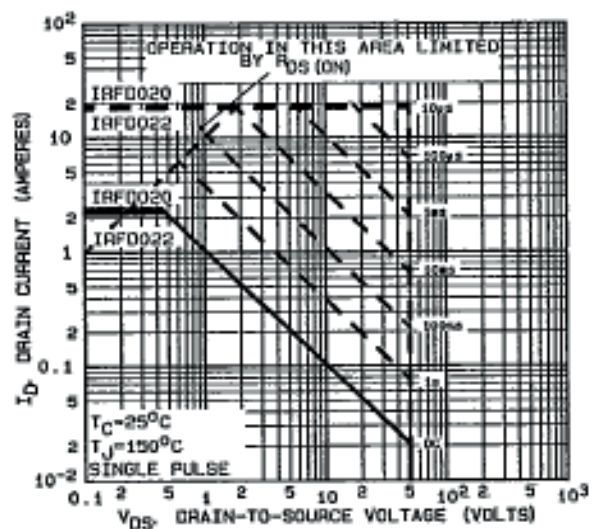


Fig. 8 - Maximum Safe Operating Area

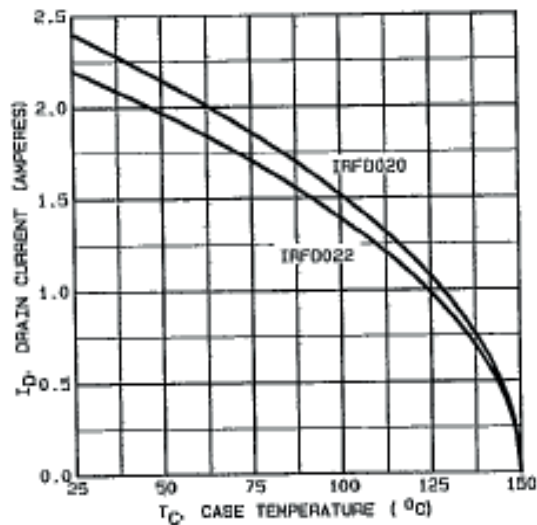


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

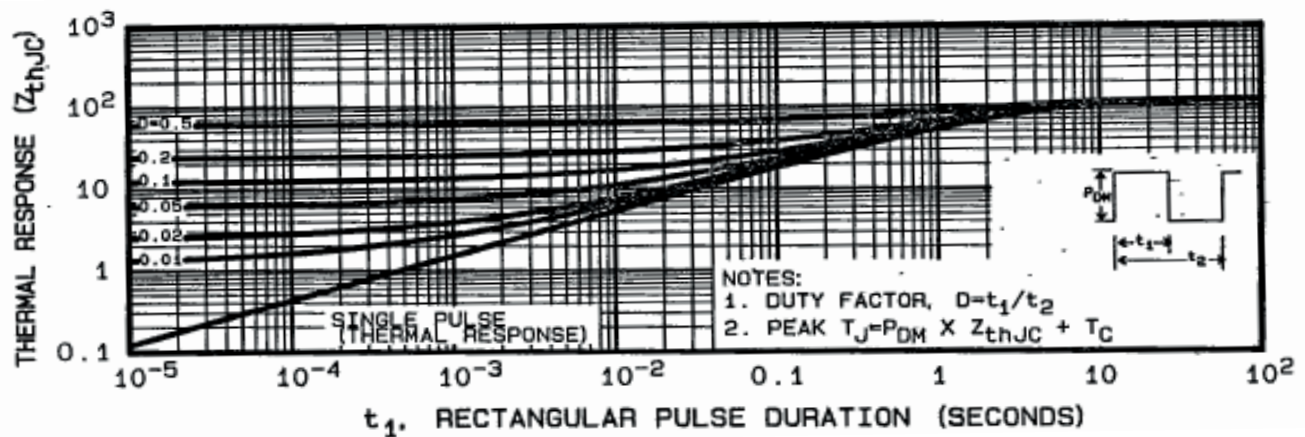


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

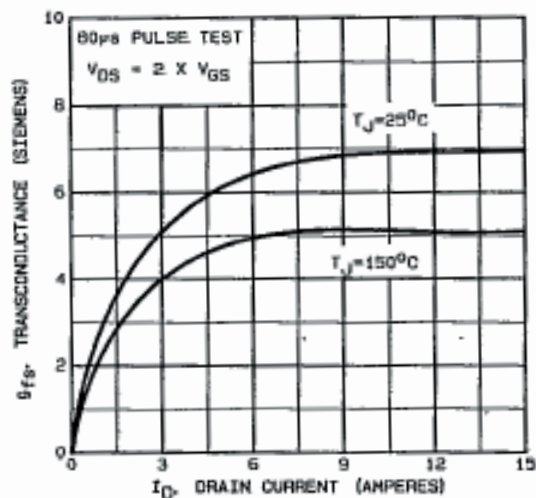


Fig. 11 - Typical Transconductance vs. Drain Current

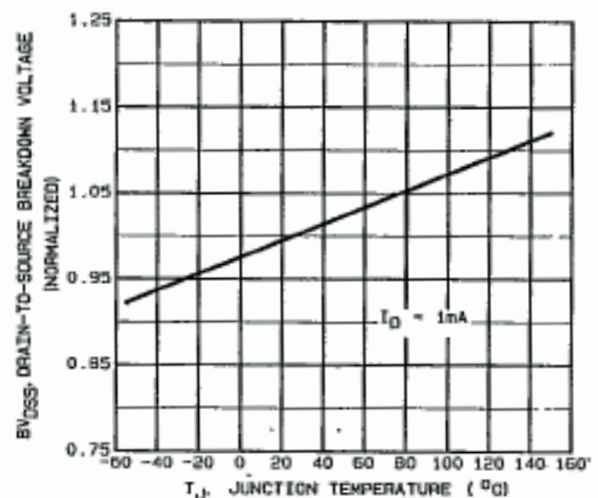
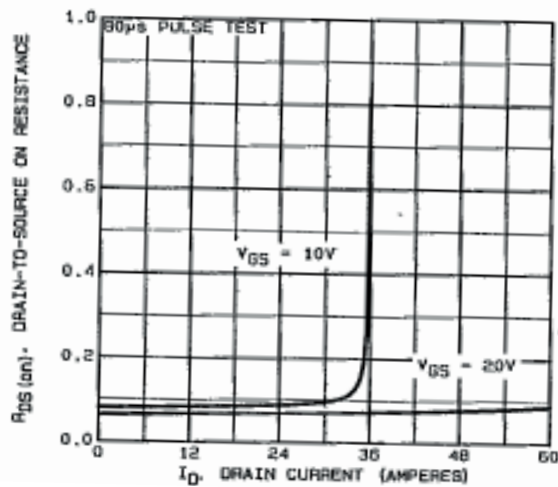
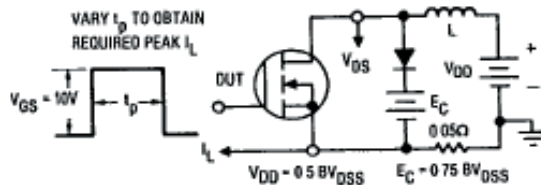
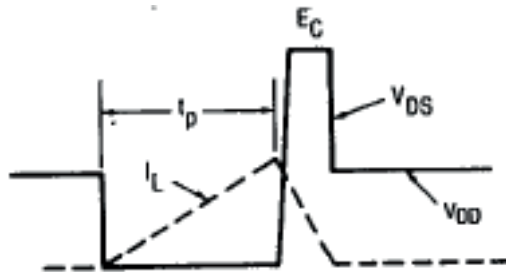
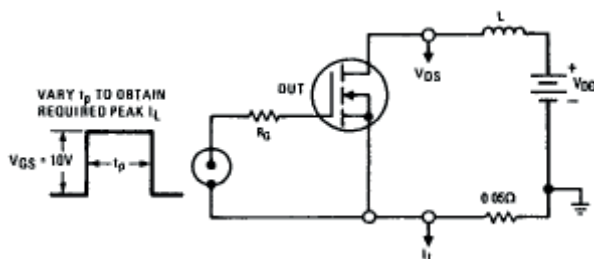
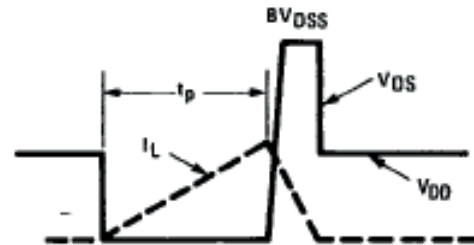
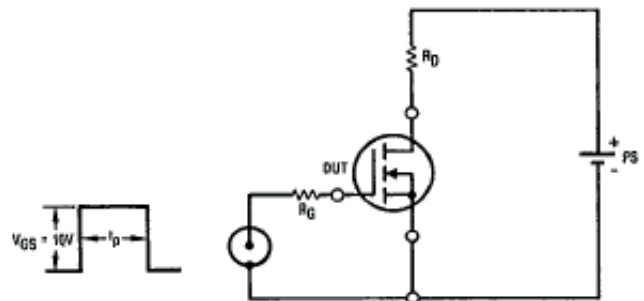
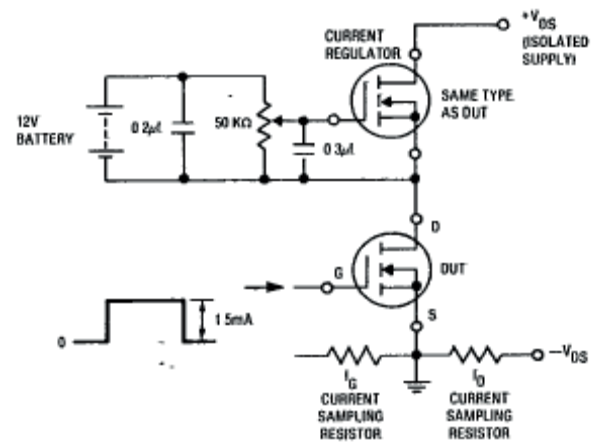


Fig. 12 - Breakdown Voltage vs. Temperature


Fig. 13 - Typical on-Resistance vs. Drain Current

Fig. 14a - Clamped Inductive Test Circuit

Fig. 14b - Clamped Inductive Waveforms

Fig. 15a - Unclamped Inductive Test Circuit

Fig. 15a - Unclamped Inductive Load Test Waveforms

Fig. 16 - Switching Time Test Circuit

Fig. 17 - Gate Charge Test Circuit

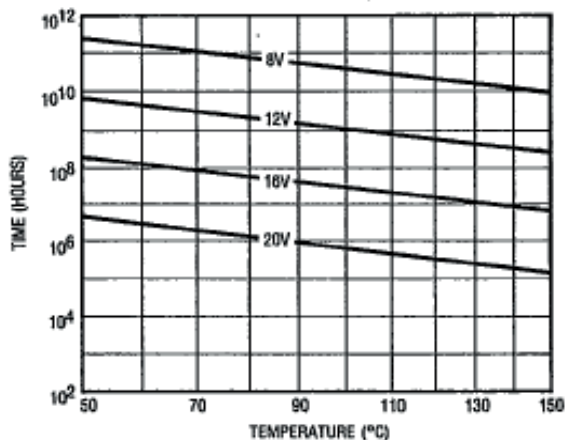


Fig. 18 - Typical Time to Accumulated 1 % Gate Failure

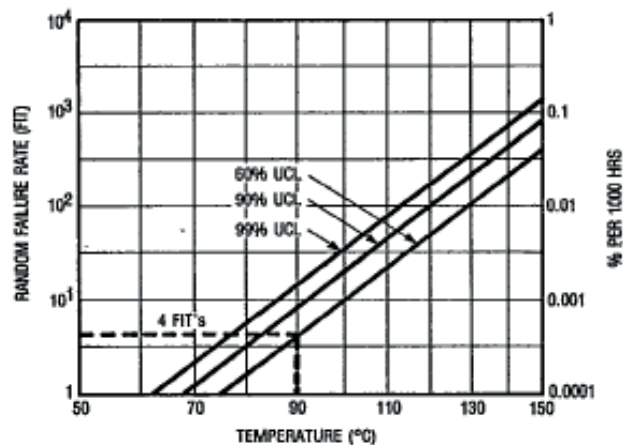
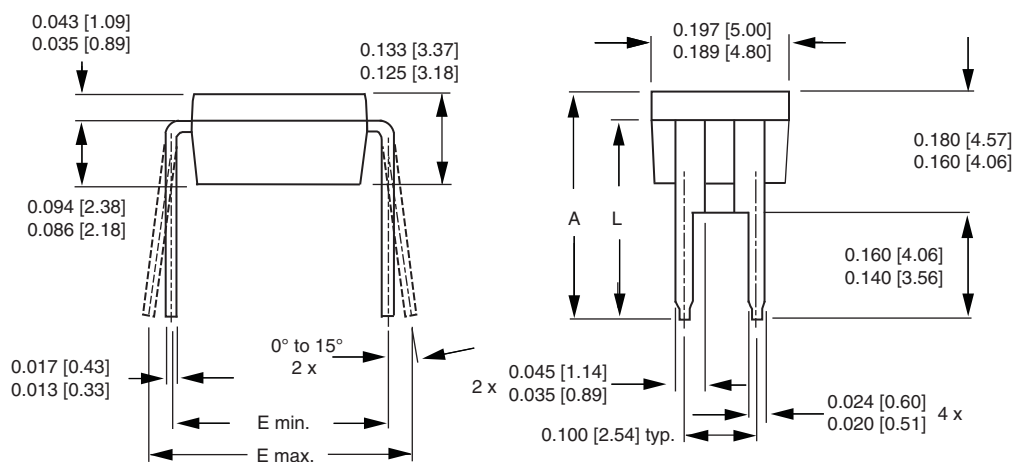


Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91465.



	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10

DWG: 5974

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Vishay products are not designed for use in life-saving or life-sustaining applications or any application in which the failure of the Vishay product could result in personal injury or death unless specifically qualified in writing by Vishay. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.