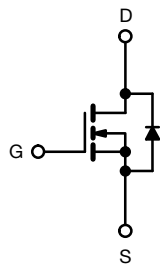
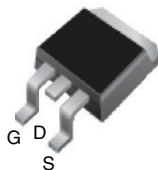


Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

PRODUCT SUMMARY

V _{DS} (V)	100
R _{DS(on)} (Ω)	V _{GS} = 5 V 0.077
Q _g max. (nC)	64
Q _{gs} (nC)	9.4
Q _{gd} (nC)	27
Configuration	Single

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- Logic-level gate drive
- R_{DS(on)} specified at V_{GS} = 4 V and 5 V
- 175 °C operating temperature
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details



RoHS*
Available
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHL540S-GE3	SiHL540STRL-GE3 ^a
Lead (Pb)-free	IRL540SPbF	IRL540STRLPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	100	V
Gate-source voltage	V _{GS}	± 10	
Continuous drain current	I _D	T _C = 25 °C 28	A
		T _C = 100 °C 20	
Pulsed drain current ^a	I _{DM}	110	W/°C
Linear derating factor		1.0	
Linear derating factor (PCB mount) ^e		0.025	
Single pulse avalanche energy ^b	E _{AS}	440	mJ
Avalanche current ^a	I _{AR}	28	A
Repetitive avalanche energy ^a	E _{AR}	15	mJ
Maximum power dissipation	P _D	T _C = 25 °C 150	W
Maximum power dissipation (PCB mount) ^e		T _A = 25 °C 3.7	
Peak diode recovery dv/dt ^c	dv/dt	5.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DS} = 25 V, starting T_J = 25 °C, L = 841 μH, R_g = 25 Ω, I_{AS} = 28 A (see fig. 12)
- I_{SD} ≤ 28 A, di/dt ≤ 170 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	40	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		100	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.12	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	2.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 10 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 5 V	I _D = 17 A ^b	-	-	0.077	Ω
		V _{GS} = 4 V	I _D = 14 A ^b	-	-	0.11	
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 17 A ^b		12	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	2200	-	pF
Output capacitance	C _{oss}			-	560	-	
Reverse transfer capacitance	C _{rss}			-	140	-	
Total gate charge	Q _g	V _{GS} = 5 V	I _D = 28 A, V _{DS} = 80 V, see fig. 6 and 13 ^b	-	-	64	nC
Gate-source charge	Q _{gs}			-	-	9.4	
Gate-drain charge	Q _{gd}			-	-	27	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, I _D = 28 A, R _g = 9.0 Ω, R _D = 1.7 Ω, see fig. 10 ^b		-	8.5	-	ns
Rise time	t _r			-	170	-	
Turn-off delay time	t _{d(off)}			-	35	-	
Fall time	t _f			-	80	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	28	A
Pulsed diode forward current ^a	I _{SM}			-	-	110	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 28 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 28 A, di/dt = 100 A/μs ^b		-	200	260	ns
Body diode reverse recovery charge	Q _{rr}			-	1.7	2.9	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

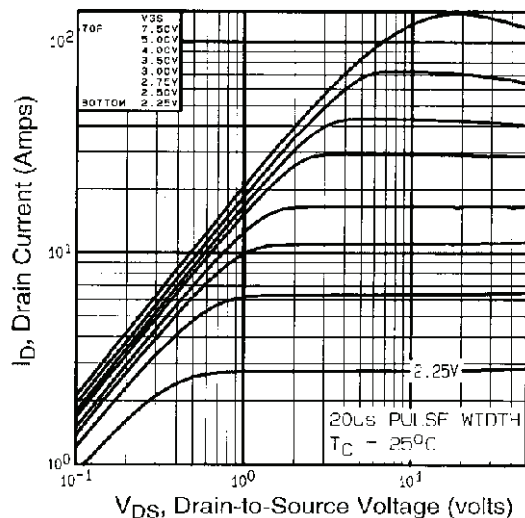


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

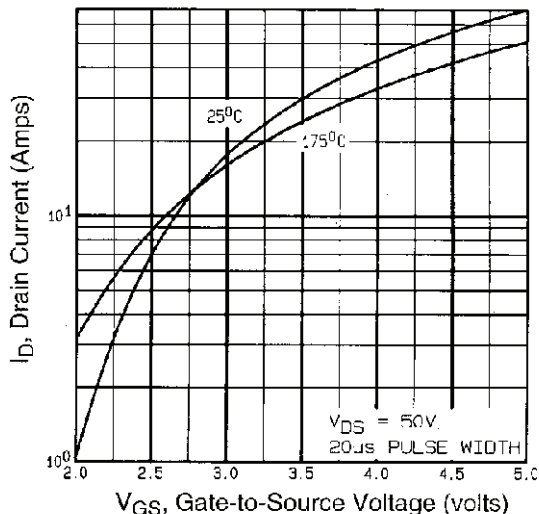


Fig. 3 - Typical Transfer Characteristics

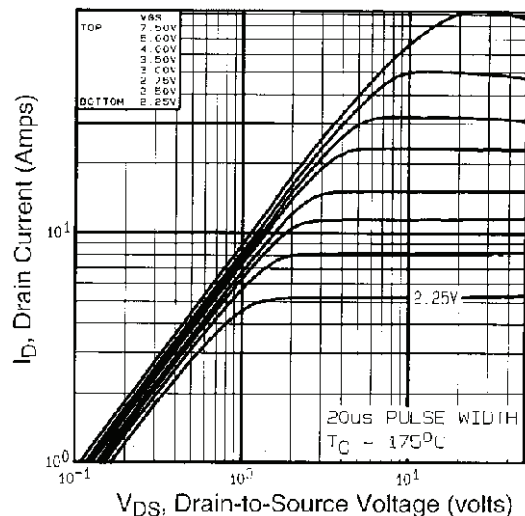


Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$

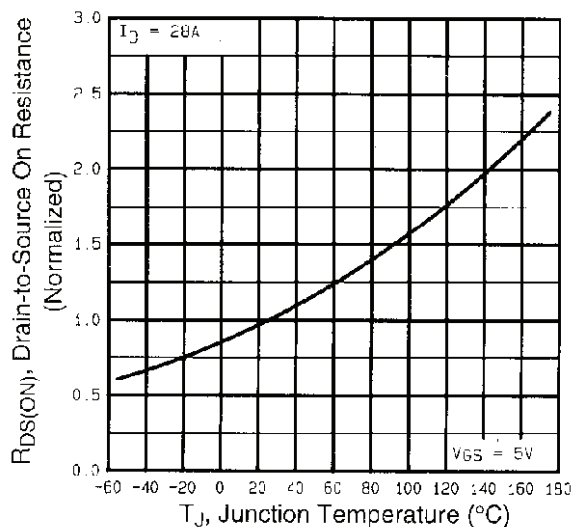
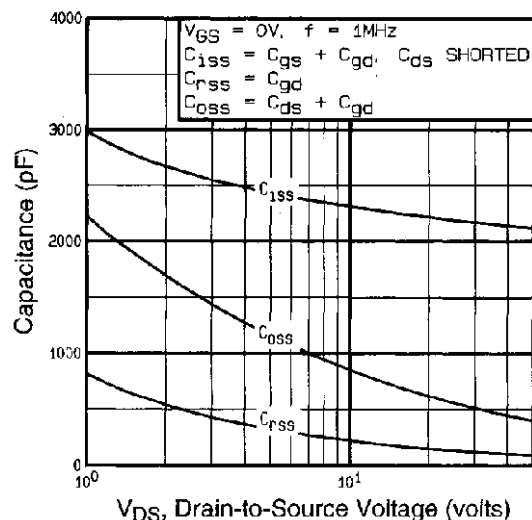
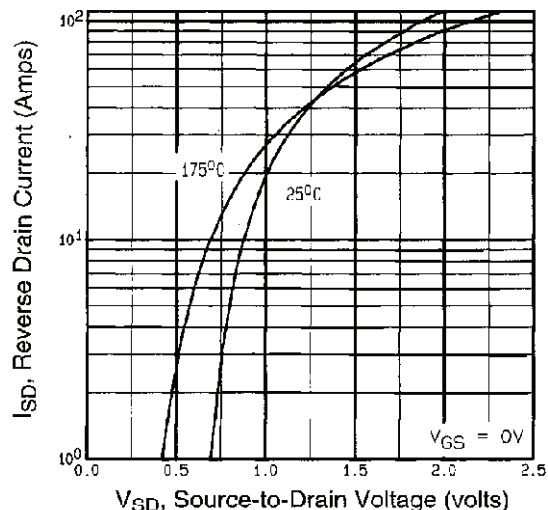
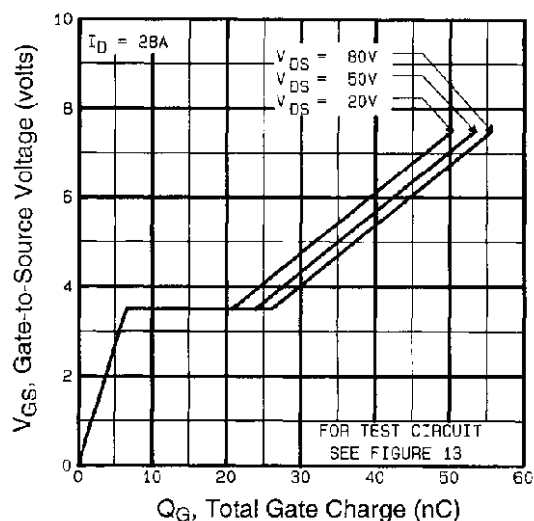
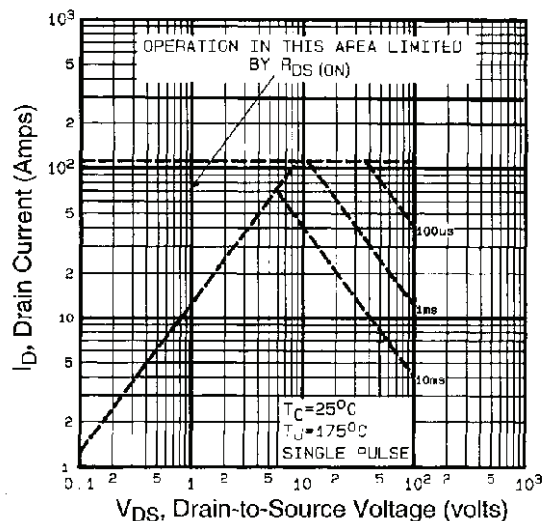
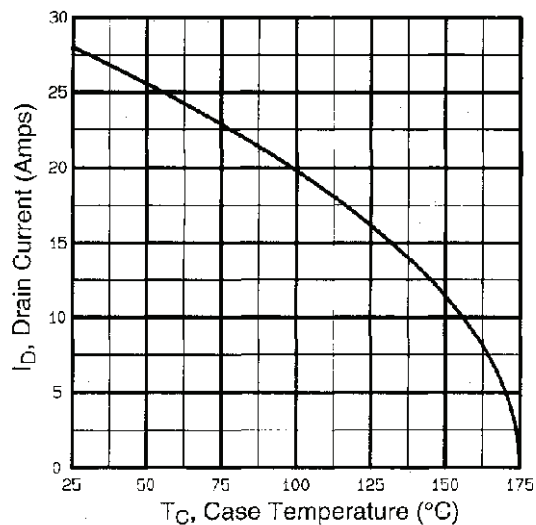
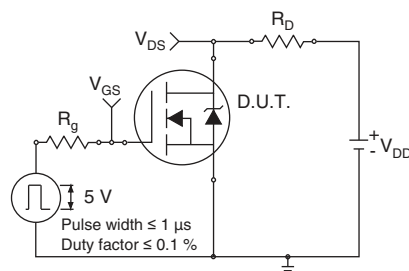
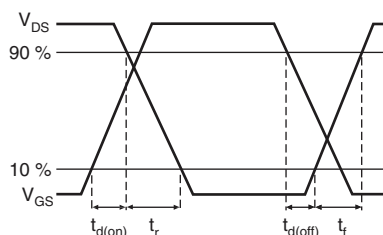
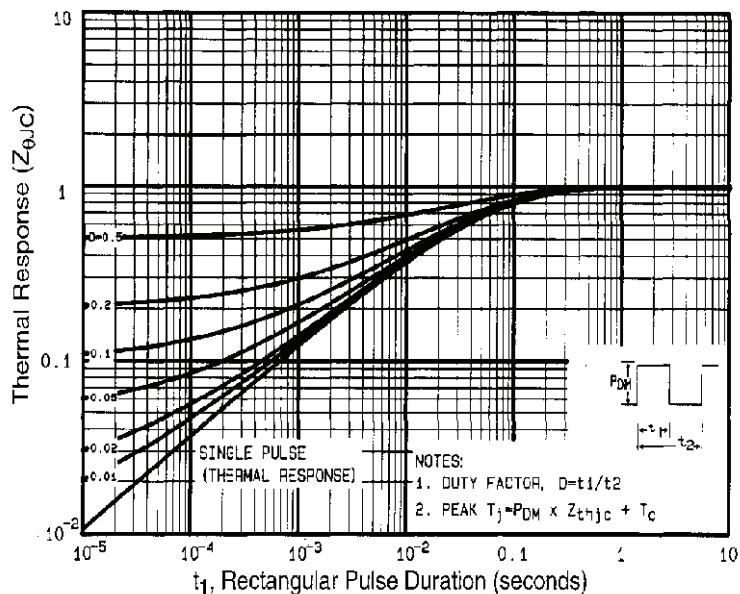
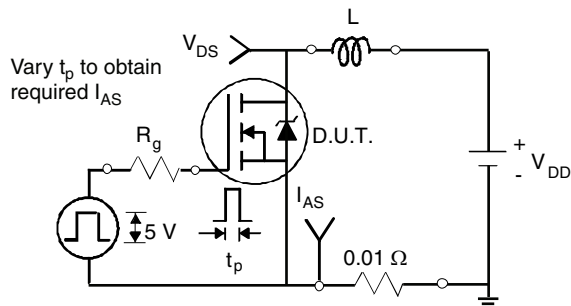
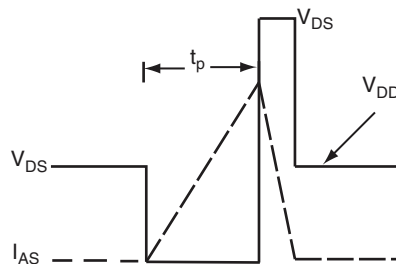


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

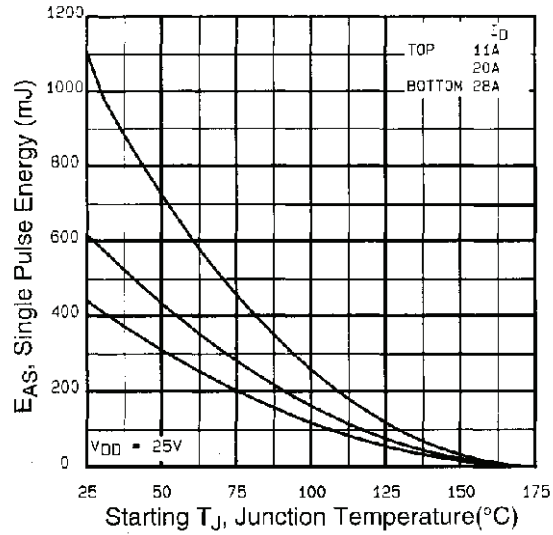


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

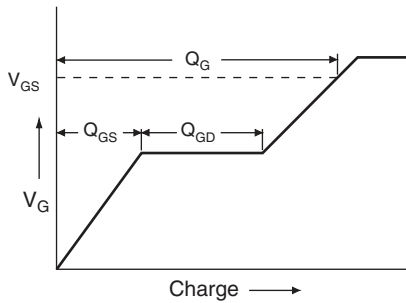


Fig. 13a - Basic Gate Charge Waveform

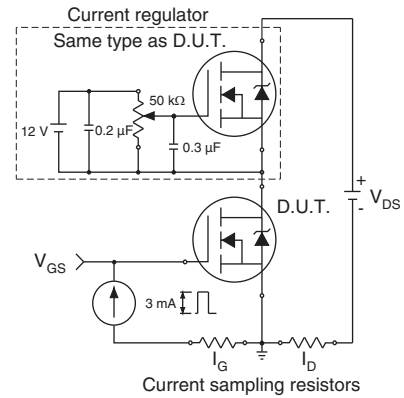
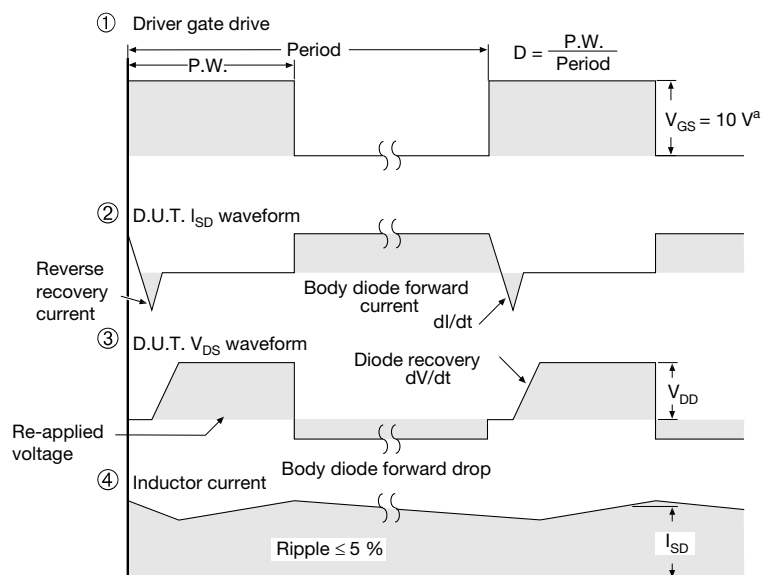
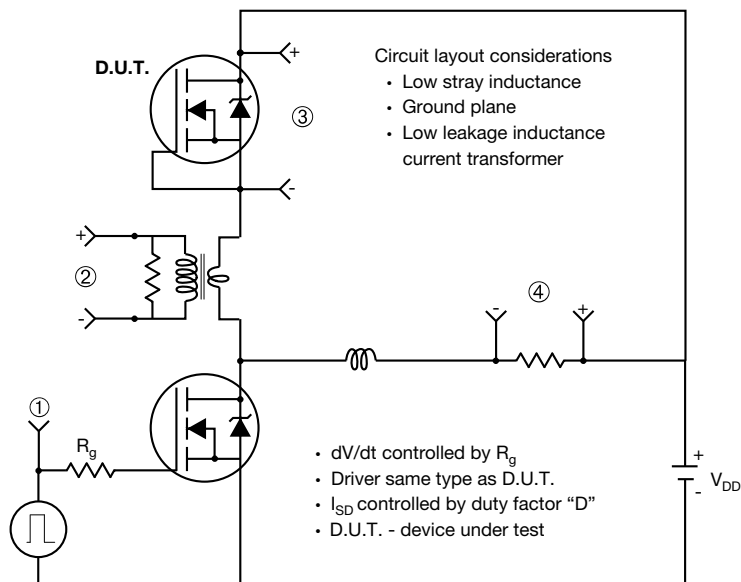


Fig. 13b - Gate Charge Test Circuit

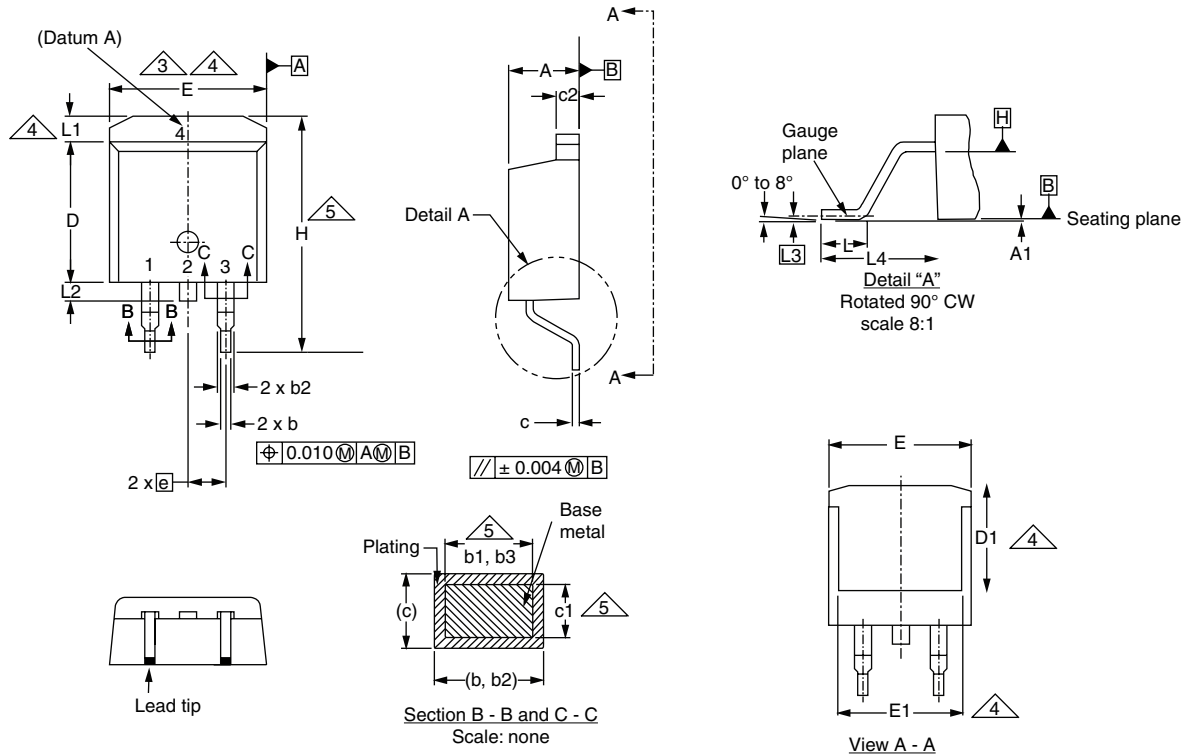
Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

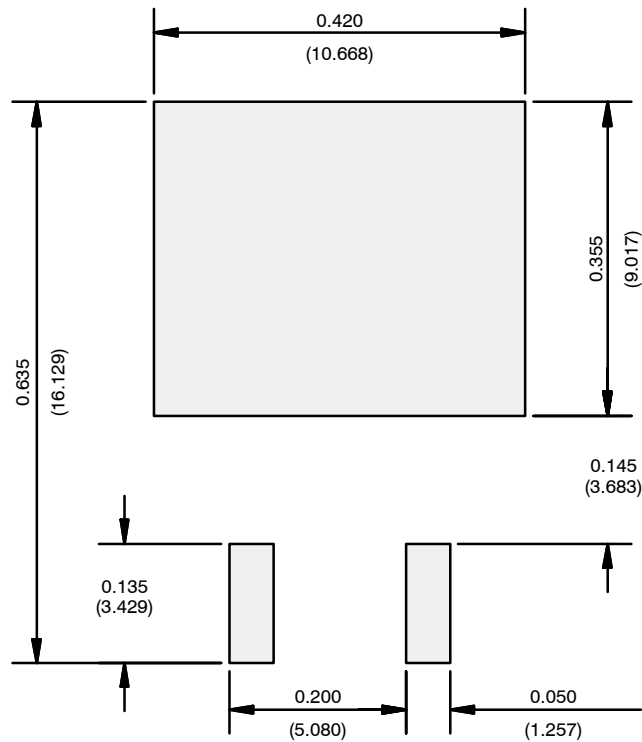
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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