USB VBUS I_{SOURCE} Load Switch with Current Limit Control

Features

- 2.5V to 5.5V Supply Voltage Range at IN
- 29V Abs. Max. Rating at OUT
  - ±80V Surge Protection (IEC61000-4-5)
  - ±8kV ESD Contact Discharge (IEC61000-4-2)
  - ±15kV ESD Air Gap Discharge (IEC61000-4-2)
- 30mΩ typ. On-Resistance from IN to OUT
- Adjustable Current Limit Protection (CLP)
  - 400mA to 3.7A via R_{ISET}
- Over-Current Protection (OCP)
- Short-Circuit Protection (SCP)
- "Ideal Diode" Reverse Current Protection (RCP)
- Over Temperature Protection (OTP)
- Soft-Start (SS) Limits Inrush Current
- Fast Turn ON supports USB Fast Role Swap (FRS)
  - Open-Drain $\overline{FLT}$ Flag
- Safety approvals
  - UL 2367, file no. E515099
- -40°C to 85°C Operating Temperature Range
- 16-bump WLCSP 1.98 x 1.98mm (0.5mm pitch)
- Pin-to-Pin with NX5P3290A & NX5P3363

Applications

- Notebooks, Ultra-Books, Desktop PCs
- Smartphones, Tablets, Gaming Consoles
- Set-Top Box, Networking, any USB I_{SOURCE} Port

Brief Description

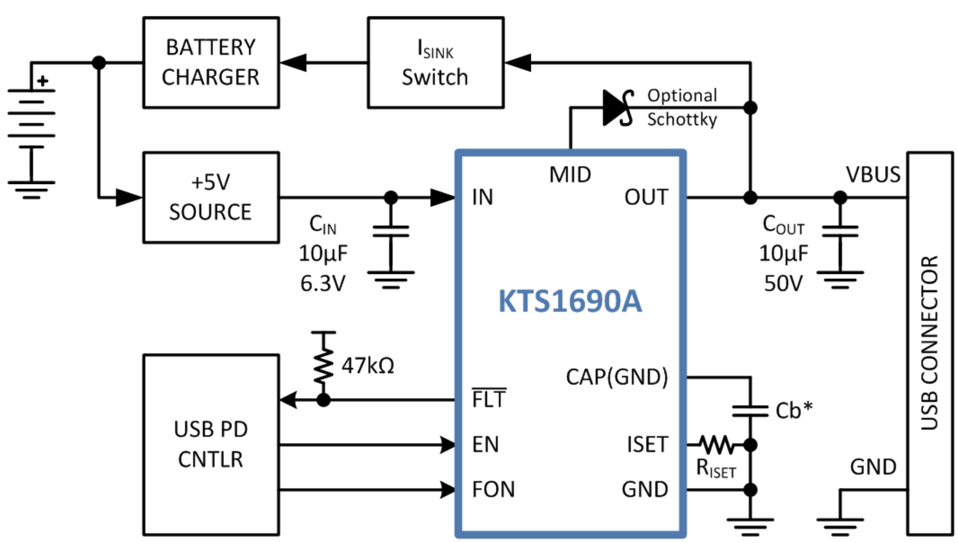
The KTS1690A is a low-resistance load switch with adjustable current limit, soft-start, fast turn ON mode, "ideal diode" reverse current protection, and integrated TVS. It is optimized to protect systems with USB type-C ports that source up to 15W at 5V and must withstand up to 29V on VBUS (OUT pin).

The KTS1690A uses an external resistor to set the current limit from 400mA to 3.7A.

Soft-start limits inrush current, while the FON logic input enables fast turn ON mode for USB fast role swap (FRS). Automatic "ideal diode" reverse current protection (RCP) isolates the system's 5V internal rail whenever VBUS (OUT pin) is driven to a higher voltage, as when charging. The integrated TVS provides IEC Standards ±8kV ESD contact, ±15kV ESD air gap, and ±80V surge ratings for robust system protection. A $\overline{FLT}$ flag indicates an over-current or over-temperature fault condition.

The KTS1690A is available in advanced, fully "green" compliant, 1.98 x 1.98mm, 16-bump Wafer-Level Chip-Scale Package (WLCSP).

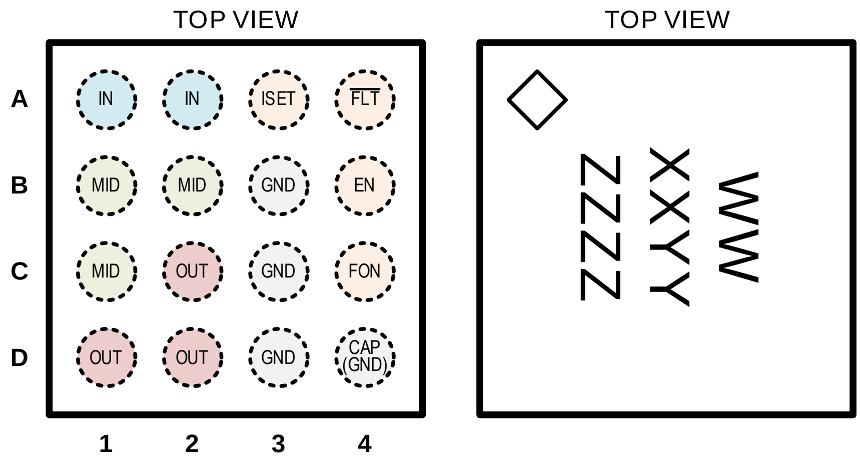
Typical Application



Cb* = optional 1nF, open, or short to GND

Pinout Diagram

WLCSP-16



16-bump 1.98mm x 1.98mm x 0.62mm
WLCSP Package, 0.5mm pitch
Top Mark
WW = Device ID,
XX = Date Code, YY = Assembly Code,
ZZZZ = Serial Number

Pin Descriptions

Pin #	Pin name	Function
A1, A2	IN	Supply Input – input to the power switches
B1, B2, C1	MID	Middle point of the power switches – Place an optional Schottky diode from MID to OUT to improve V_{OUT} droop during load-transients and RCP recovery.
C2, D1, D2	OUT	Output of the power switches
B3, C3, D3	GND	Ground
A3	ISET	Current Limit Setting – Adjust the current limit using a resistor from ISET to GND.
A4	$\overline{FLT}$	Fault Logic Output – active-low, open-drain flag indicates current limit protection (CLP) and over temperature (OT) faults
B4	EN	Enable Logic Input – active-high with internal 1MΩ pull down
C4	FON	Fast Turn-On Logic Input – active-high with internal 1MΩ pull down
D4	CAP (GND)	Internally connected to GND. Optionally leave floating (N.C.) or optionally connect a 1nF capacitor from CAP to GND for pin-to-pin PCB layouts.

Ordering Information

Part Number	Marking[1]	Operating Temperature	Package
KTS1690AEGAA-TA	NIXXYYZZZZ	-40°C to +85°C	WLCSP44-16

1. WW = Device ID, XX = Date Code, YY = Assembly Code and ZZZZ = Serial Number.

Absolute Maximum Ratings[2]

Symbol	Description	Value	Units
V_{OUT}	OUT to GND (continuous)	-0.3 to 29	V
	OUT to GND (during IEC61000-4-5 ±80V surge event, 20µs pulse)	-5 to 38	
V_{IN}, V_{MID}, V_{ISET}	IN, MID, ISET to GND	-0.3 to 6.0	V
V_I, V_O	EN, FON, $\overline{FLT}$ to GND	-0.3 to 6.0	V
V_{CAP}	CAP to GND	-0.01 to 0.01	V
I_{SW}	Maximum Continuous Switch Current[3]	4	A
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[4]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (OUT)	±8	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (OUT)	±15	kV
V_{SURGE}	IEC61000-4-5 Surge (OUT to GND)	±80	V

Thermal Capabilities[5]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	80	°C/W
P_D	Maximum Power Dissipation at T_A = 25°C	1.25	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-12.5	mW/°C

Recommended Operating Conditions[6]

Symbol	Description	Value	Units
V_{OUT}	Output Voltage	0 to 24	V
V_{IN}	Input Supply Voltage	2.5 to 5.5	V
V_I, V_O	Logic Input and Output Voltage	0 to 5.5	V
I_{SW}	Switch Current	0 to 3.3	A
R_{ISET}	Current Limit Setting Resistance	14.3 to 140	kΩ
C_{OUT}	Output Capacitance	1 to 100	µF
T_A	Ambient Operating Temperature	-40 to 85	°C

2. Stresses above those listed in Absolute Maximum Ratings (AMR) may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one AMR should be applied at any one time.

3. Internally limited

4. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may performance better than specified.

5. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

6. The Recommended Operating Conditions table defines the conditions for actual device operation and are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to the Abs. Max. Ratings.

Electrical Characteristics[7]

Unless otherwise noted, the Min and Max specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C and V_{IN} = 5.0V.

Symbol	Description	Conditions	Min	Typ	Max	Units
Supply Specifications (IN)						
V_{IN}	Input Supply Voltage Operating Range		2.5		5.5	V
V_{UVLO}	Under-Voltage Lockout	V_{CC} rising threshold	2.12	2.3	2.48	V
		Hysteresis		100		mV
I_Q	No-Load Supply Current	Enabled, EN = 1, FON = 0		220	320	µA
I_{Q_FON}		Enabled, EN = 1, FON = 1		220	320	µA
I_{SHDN}		Shutdown, EN = 0		3.5	10	µA
Thermal Shutdown Specifications						
T_{J_SHDN}[8]	IC Junction Thermal Shutdown	T_J rising threshold		150		°C
		Hysteresis		25		°C
Logic Pin Specifications (EN, FON, $\overline{FLT}$)						
V_{IH}	Input Logic High Voltage	EN, FON pins	1.2			V
V_{IL}	Input Logic Low Voltage	EN, FON pins			0.4	V
R_{I_PD}	Input Logic Pull-Down	EN, FON pins	0.72	1		MΩ
V_{OL}	Output Logic Low	$\overline{FLT}$ pin, I_{O_SINK} = 4mA		0.02	0.3	V
I_{O_LK}	Output Logic Leakage	$\overline{FLT}$ pin, T_A = 25°C, V_O = V_{IN}		0.01	1	µA
Switch Specifications (IN, OUT)						
R_{ON}	On Resistance (IN to OUT)	V_{IN} = 5V, T_A = 25°C		30	42	mΩ
		V_{IN} = 5V, T_A = -40°C to 85°C			49	
		V_{IN} = 3.7V, T_A = 25°C		30	44	
		V_{IN} = 3.7V, T_A = -40°C to 85°C			51	
$I_{LK(OFF)}$	Off Leakage Current (at OUT pin)	V_{IN} = 5V, V_{OUT} = 0V, EN = 0		0.003		µA
		V_{OUT} = 5V, V_{IN} = 0V, EN = 0		0.03	1	
		V_{OUT} = 20V, V_{IN} = 0V, EN = 0		0.11	3	
$I_{LK(RCP)}$	RCP Bias Current	V_{OUT} = 20V, V_{IN} = 5V, EN = 1		10	15	µA
I_{CLP}	Current Limit Protection	V_{IN} = 3.7V to 5.5V, R_{ISET} = 51kΩ	915	1013	1107	mA
		V_{IN} = 3.7V to 5.5V, R_{ISET} = 31.6kΩ	1505	1650	1780	
		V_{IN} = 3.7V to 5.5V, R_{ISET} = 30kΩ[8]	1585	1738	1875	
		V_{IN} = 3.7V to 5.5V, R_{ISET} = 16kΩ[8]	3100	3300	3531	
		V_{IN} = 3.7V to 5.5V, R_{ISET} = 14.3kΩ[8]	3468	3692	3951	
		V_{IN} = 3.7V to 5.5V, V_{ISET} = V_{IN}	168	210	273	
I_{CLP_SS}	Soft-Start Current Limit Protection for SCP	FON = 0		1.2		A
		FON = 1		n/a		
V_{SCP_SS}	Short-Circuit Protection Threshold in Soft-Start	V_{OUT} < V_{SCP_SS} at end of SS		0.4V_{IN}		V
I_{OCP}	Over Current Protection Threshold for SCP			5.8		A
V_{REG_RCP}	"Ideal Diode" RCP V_{OUT} Droop Regulation Voltage	V_{IN} – V_{OUT}, V_{IN} = 3.7V to 5.5V		60		mV

7. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

8. Guaranteed by design, characterization and statistical process control methods; not production tested.

Electrical Characteristics (continued)[7]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C and V_{IN} = 5.0V.

Symbol	Description	Conditions		Min	Typ	Max	Units
TVS Surge Clamp Specifications (OUT)							
V_{OUT_WRK}	Output Clamp Working Voltage	Positive Working Voltage				29	V
		Negative Working Voltage		0			
V_{OUT_CLMP}	Output Clamp Breakdown Voltage	I_{OUT} = 10mA, T_A = 25°C			31		V
		I_{OUT} = -10mA, T_A = 25°C			-0.6		
V_{OUT_SRG}	Output Clamp Surge Voltage	+80V surge, T_A = 25°C			33		V
		-80V surge, T_A = 25°C			-2		
Timing Specifications, see Figure 1							
t_{DON}	Turn-On Delay	R_L = 100Ω, C_L = 10µF	FON = 0		0.75		ms
			FON = 1		30	50	µs
t_R	V_{OUT} Rise Time		FON = 0		1.5		ms
			FON = 1		50	100	µs
t_{DOFF}	Turn-Off Delay	R_L = 100Ω, C_{OUT} = 10µF			70		µs
t_F	V_{OUT} Fall Time (Strictly R_L & C_{OUT} dependent)				3		ms
$t_{D\overline{FLT}}$	$\overline{FLT}$ Flag Trigger Delay Time	CLP event to $\overline{FLT}$ = 0			8		ms
$t_{RD\overline{FLT}}$	$\overline{FLT}$ Flag Recovery Delay Time	CLP/OT event recovery to $\overline{FLT}$ = high-Z			17		ms
t_{RCP}	RCP Response Time	Trigger (V_{OUT} > V_{IN})			2		µs
		Recovery (V_{OUT} < V_{IN} – 60mV)			15		
t_{OCP}	Over Current Protection Response Time				1		µs
t_{SCP_SS}	Short-Circuit Detection Time during Soft-Start	V_{OUT} < $0.4V_{IN}$			7		ms
t_{HICCUP}	Short-Circuit Hiccup Retry Time				70		ms
t_{FON_BLNK}	Fast Turn-On CLP Blanking Time	FON = 1, time from EN going high until CLP is active			370		µs

Timing Diagrams

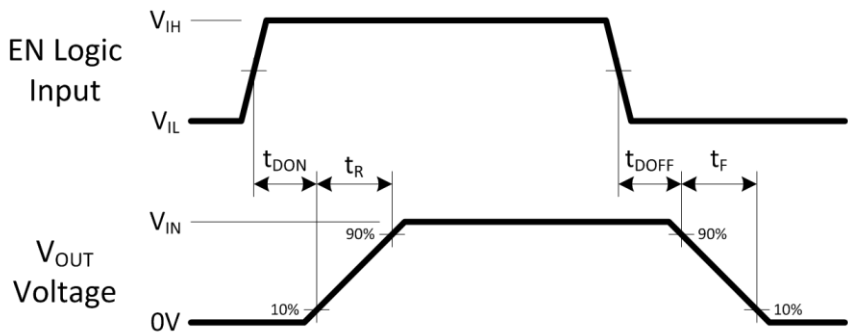
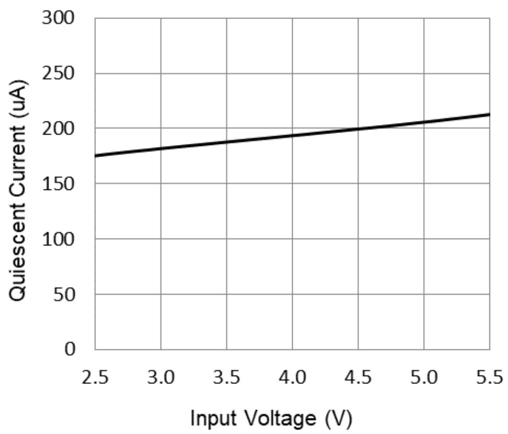


Figure 1. On/Off Timing Diagram

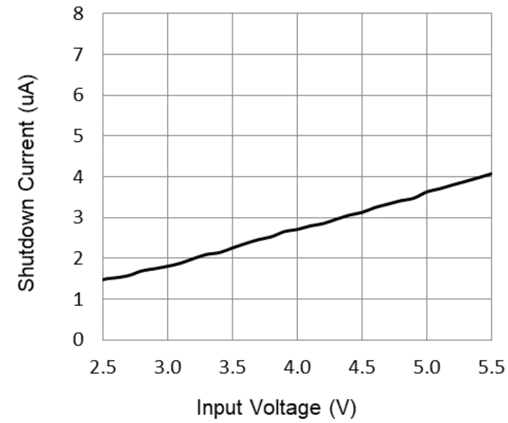
Typical Characteristics

V_{IN} = 5.0V, FON = Low, C_{IN} = 10µF, C_{OUT} = 10µF, R_{ISET} = 16kΩ (3.3A CLP), T_A = 25°C, unless otherwise specified.

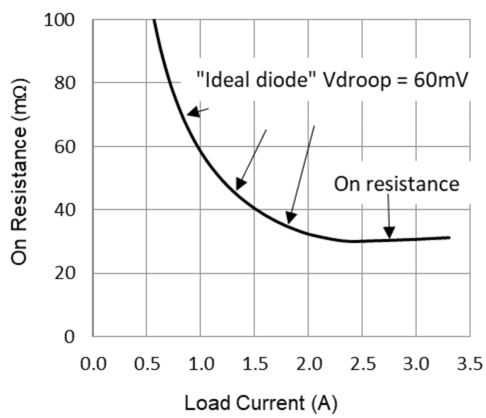
No-Load Supply Current vs. VIN
(EN = High)



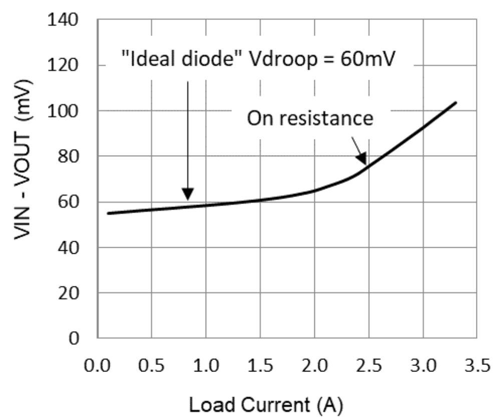
Shutdown Supply Current vs. VIN
(EN = Low)



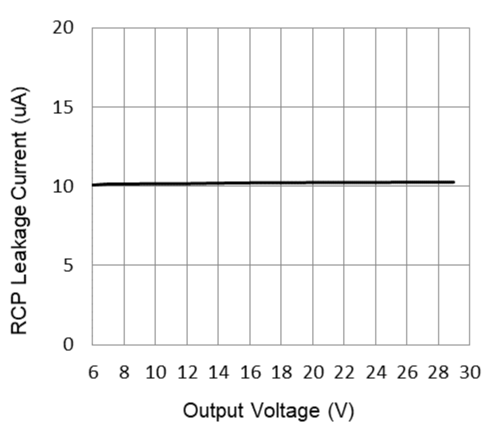
On Resistance vs. Load Current
(VIN = 5V)



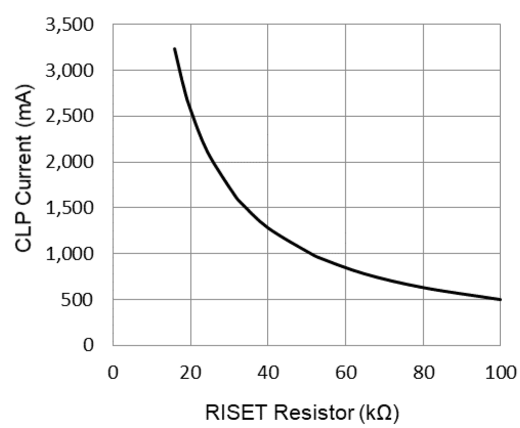
"Ideal diode" Vdroop vs. Load Current
(VIN = 5V)



RCP Bias Current vs. VOUT
(VIN = 5V, EN = H)



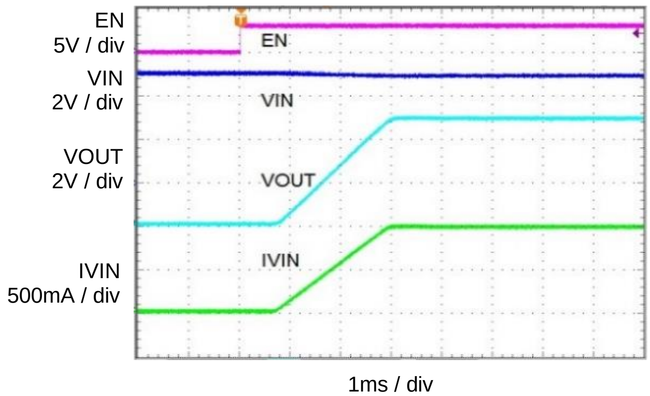
CLP Current vs. R_{ISET} Resistor



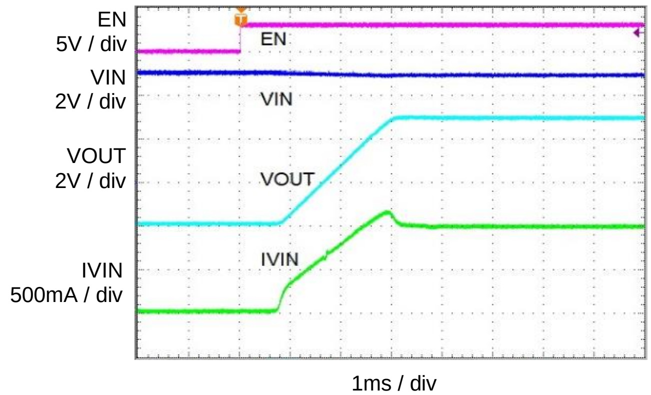
Typical Characteristics

V_{IN} = 5.0V, FON = Low, C_{IN} = 10µF, C_{OUT} = 10µF, R_{ISET} = 31.6kΩ (1.65A CLP), T_A = 25°C, unless otherwise specified.

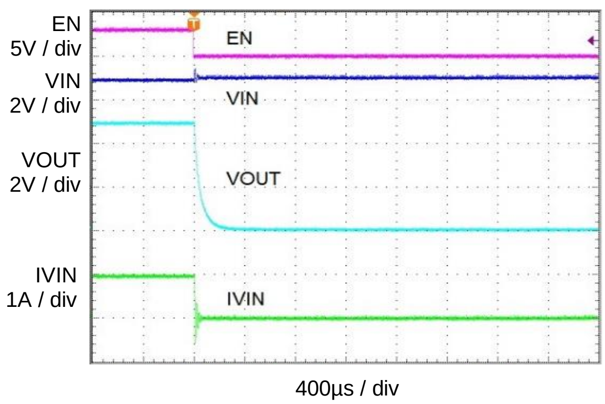
Turn On by Enable
(C_{OUT} = 10µF, R_L = 5Ω)



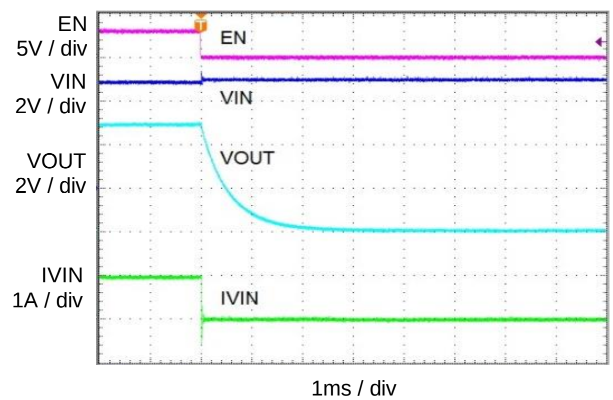
Turn On by Enable
(C_{OUT} = 10+100µF, R_L = 5Ω)



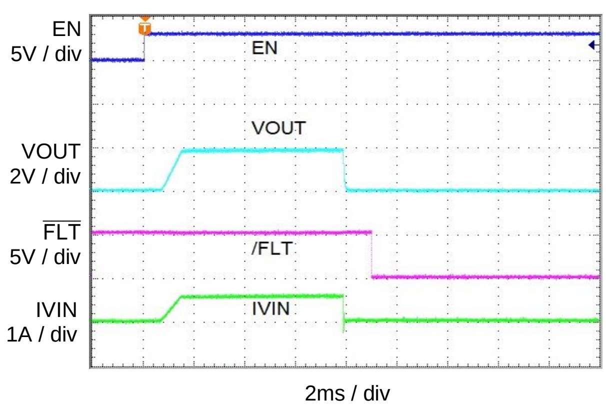
Turn Off by Enable
(C_{OUT} = 10µF, R_L = 5Ω)



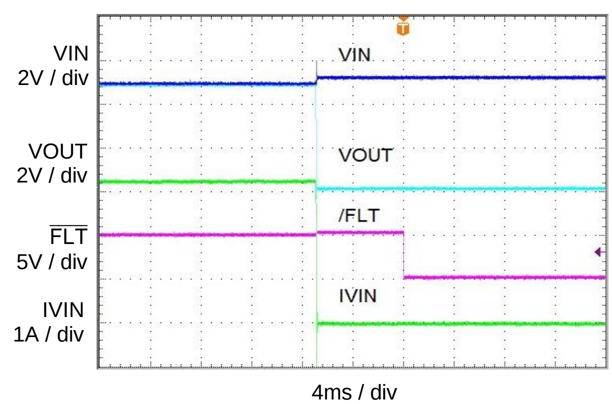
Turn Off by Enable
(C_{OUT} = 10+100µF, R_L = 5Ω)



Device Enabled into Current Limit Mode
(1.6A CLP)



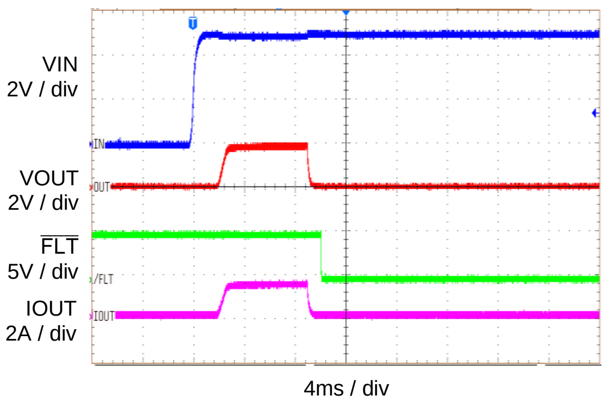
Load Increase Trigger Current Limit
(3.3A CLP)



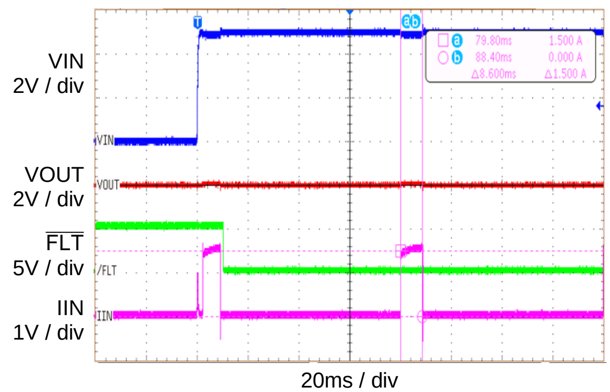
Typical Characteristics

V_{IN} = 5.0V, FON = Low, C_{IN} = 10µF, C_{OUT} = 10µF, R_{ISET} = 31.6kΩ (1.65A CLP), T_A = 25°C, unless otherwise specified.

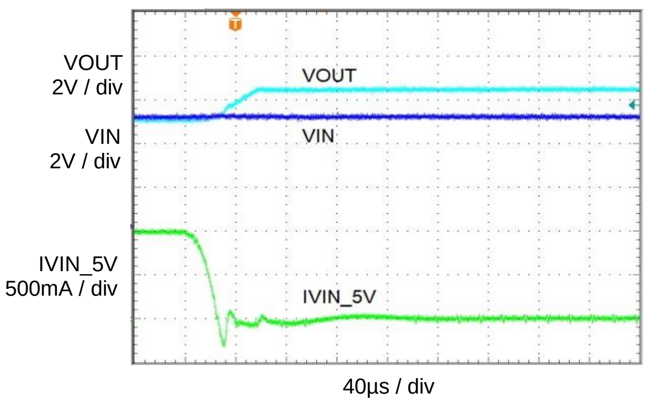
Start-Up into VBUS Short to GND
(R_{ISET} = 14.3K)



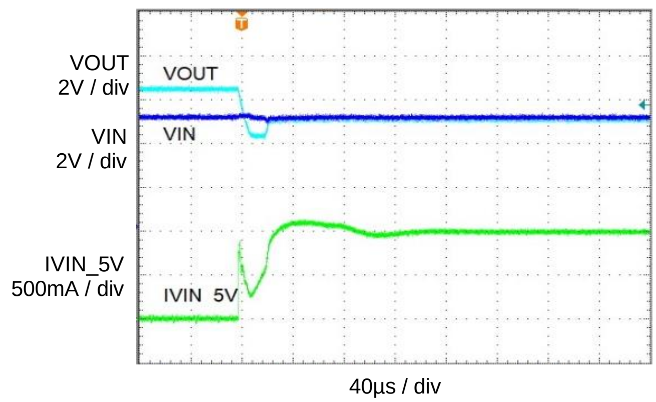
Start-Up into VBUS Short with Hiccup Retry
(R_{ISET} = 14.3K)



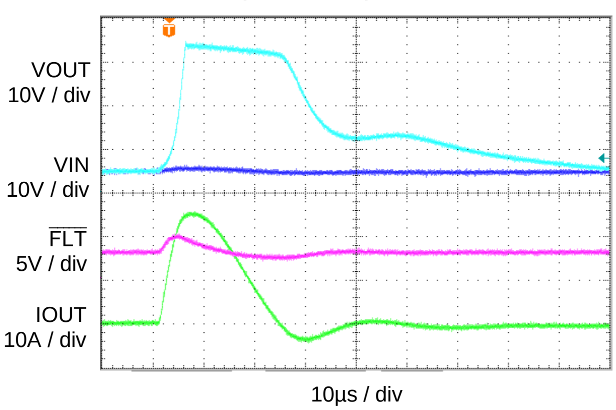
Reverse Current Protection Trigger
(VOUT rising to 7V, C_{IN} = 20 + 100µF, R_L = 5Ω)



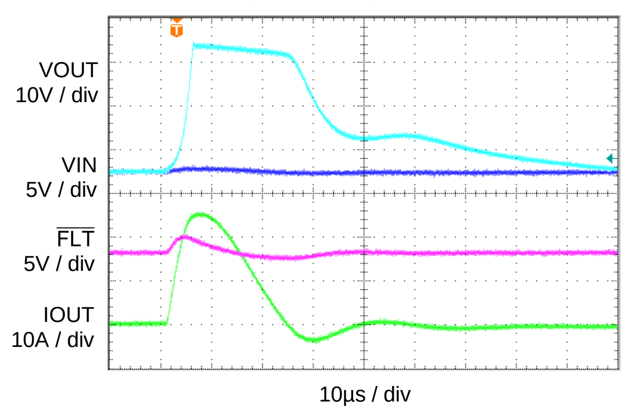
Reverse Current Protection Recovery
(VOUT falling to 5V, C_{IN} = 20 + 100µF, R_L = 5Ω)



VOUT Surge Response +80V
(VIN = 5V)



VOUT Surge Response -80V
(VIN = 5V)



Functional Block Diagram

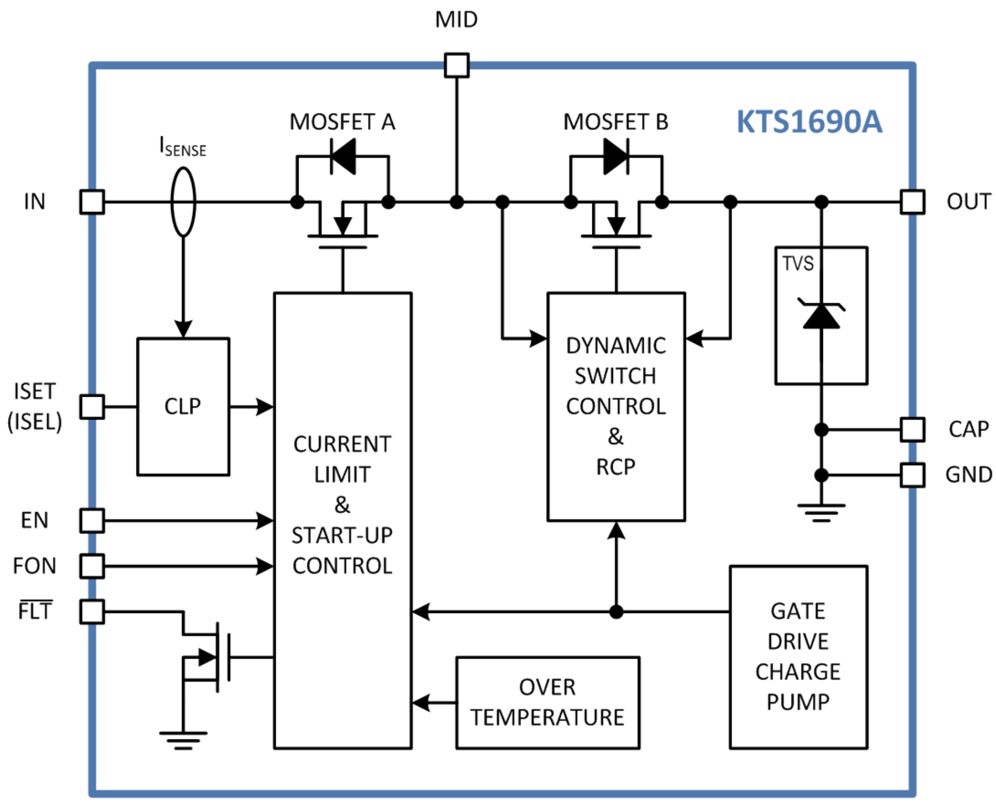


Figure 2. Functional Block Diagram

Functional Description

The KTS1690A is a 30mΩ (typ) low resistance power switch intended to be inserted between a power source and a load to isolate and protect against ESD, surge, and excessive voltage and load-current conditions at the output. It features slew-rate controlled turn ON (soft-start) to prevent input voltage droop resulting from a large inrush current when starting into capacitive loads. For USB fast role swap applications, the fast turn-on feature speeds up soft-start when the FON pin is set to logic 1. The KTS1690A also features several additional protection functions, such as output surge and ESD protection, output current limit protection, output short-circuit protection, input under-voltage lockout, reverse current protection, and over-temperature protection. KTS1690A operates over a wide input voltage range of 2.5V to 5.5V, and its output is designed to withstand up to 29V continuously and up to 38V during IEC61000-4-5 ±80V surge events (whether in shutdown or enabled).

Shutdown and Enable

When EN is set to logic 0, the main power MOSFETs are disabled, and the device enters low-power shutdown mode. During shutdown mode, the output ESD and surge clamp continue to protect the IC and system. When EN is set to logic 1, all additional protection circuits are enabled, and if no fault condition exists, the main power MOSFETs are turned ON.

Under-Voltage Lockout (UVLO)

The UVLO function keeps the switches in the OFF state when the input voltage is below the UVLO threshold, regardless of the EN logic level. When the input voltage is above the UVLO threshold and EN is set to logic 1 and there are no fault conditions, the switches are enabled to the ON state.

Slew-Rate Controlled Turn ON (Soft-Start)

The KTS1690A has slew-rate control during normal startup for suppressing inrush current. The V_{OUT} turn-on delay is 0.75ms (typ), and then the V_{OUT} rise time is 1.5ms (typ) for a total start-up time of 2.25ms (typ).

Fast Turn ON

To support USB power delivery (PD) fast role swap (FRS), set the FON pin to logic 1. With FON = 1, the turn-on delay is reduced to 50µs (max), and the rise time is reduced to 100µs (max). There are two start-up sequences for fast turn ON:

1. If $V_{OUT} < V_{IN}$, when EN goes high, the switch performs a Fast Turn ON, and the switch turns ON within 150µs (max).
2. If $V_{OUT} > V_{IN}$, even though EN is high, the switch enters RCP mode and remains OFF. Later when V_{OUT} returns below V_{IN}, the RCP recovery turns ON the switch within 50µs (max).

Note that during a Fast Turn ON, inrush current is much higher than during slew-rate controlled turn ON. For this reason, increase C_{IN} to 10µF or more as close to the IN pin as possible.

Dynamic Switch Control "Ideal Diode"

When the switch is turned ON, the KTS1690A dynamically adjusts MOSFET B's gate drive voltage to regulate the voltage droop from IN to OUT to 60mV. At light loads, the gate drive is reduced to maintain the 60mV from IN to OUT. The droop-regulation inherently provides automatic entry and exit from the reverse current protection (RCP) mode.

Dropout

During heavy load conditions, the R_{ON} of the switches may cause more than 60mV droop, but the Dynamic Switch Control then drives the gate until the switch is fully turned ON to keep the dropout as low as possible. Dropout typically occurs when the load is greater than 60mV/30mΩ = 2A.

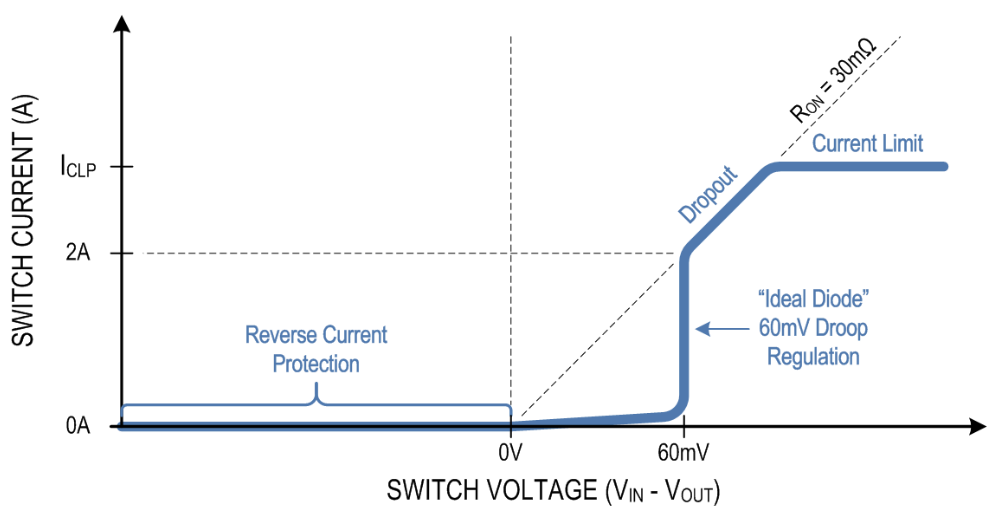


Figure 3. Switch Current vs. Switch Voltage for Dynamic Switch Control, Dropout, CLP, and RCP

Current Limit Protection (CLP)

Program the current limit using an external resistor, R_{ISET}, connected between the ISET and GND pins. See the *Switch Specifications* within the *Electrical Characteristics* table and the *CLP Current vs R_{ISET} Resistor* graph in the *Typical Characteristics* section. Calculate R_{ISET} (Ohm) for the desired nominal current limit I_{CLP} (A) per the following equation:

$$R_{ISET} = \frac{53360}{(I_{CLP} + 0.035)}$$

Whenever the switch current reaches the programmed current limit, the current limit regulation loop takes control and reduces the gate drive to limit the switch current. During CLP, the switch acts as a constant current source, and the output voltage reduces depending on the load current. Once the load current reduces below the current limit, the output voltage rises again until the Dynamic Switch Control takes over again. During CLP events, power dissipation increases, causing the die to heat up and possibly enter thermal shutdown. When the chip temperature cools, the device recovers and turns back ON.

Over-Current Protection (OCP)

During a sudden output short-circuit to ground event, switch current may ramp up very quickly, faster than the bandwidth of the CLP regulation loop. For this reason, the KTS1690A includes an additional over-current protection circuit (OCP). If the switch current exceeds the over-current threshold, OCP turns OFF the switch very quickly with <1µs (typ) response time. Once off, the switch is turned back ON via soft-start.

Short-Circuit Protection (SCP)

The OCP function provides protection for short-circuit events that occur while the switch is already enabled. But for starting into a pre-existing short at the output, the KTS1690A includes additional short-circuit protection (SCP) circuitry. During normal turn-on (FON = 0), the current limit is held to 1.2A for 7ms. Additionally, if the V_{OUT} fails to rise above 40% of V_{IN}, the switch is turned off, but automatically retries after the 70ms hiccup time.

CLP and SCP Use Cases

There are four use-cases for current limiting:

1. Turn ON into large capacitive load – during normal soft-start with very large capacitive loads, the slew-rate control may not be enough to prevent the switch current from reaching its programmed current limit. In this case, the output voltage does rise, but the soft-start current limit may extend the V_{OUT} rise time. Usually, the extended rise-time is too short to trigger thermal shutdown.
2. Turn ON into an output short-circuit to ground fault – if the output is already shorted to ground prior to start up, then V_{OUT} does not rise when EN is set to logic 1. In this case, the switch current is limited to 1.2A, and the IC dissipates significant power, $P_D = V_{IN} \times I_{CLP\_SS}$, making thermal shutdown more likely. After 7ms, if thermal shutdown has not occurred, and V_{OUT} remains below $0.4V_{IN}$, the SCP detection turns off the switch. After a 70ms hiccup time to allow the IC to cool, the soft-start retries.
3. OUT over-current event while already enabled – if the load current exceeds the current limit while the switch is already ON, then the switch current is limited to the programmed CLP current level and the output voltage sags. As V_{OUT} sags, most loads typically reduce their current requirements, so V_{OUT} usually settles at an intermediate voltage without complete collapse. The power dissipation, $P_D = (V_{IN} – V_{OUT\_SAG}) \times I_{CLP}$, is less than during an output short-circuit fault condition, so thermal shutdown is less likely, but still possible.
4. OUT short-circuit fault while already enabled – if the output is suddenly shorted to ground while the switch is already ON, then the switch current may rise very rapidly and temporarily exceed the programmed CLP current limit.
    a. If the switch current reaches the OCP current threshold, the switch is turned OFF very quickly, and then restarted as in use-case 2 above.
    b. If the switch current does not reach the SCP current threshold quickly, then the CLP control loop reduces the switch current to the programmed current level. In this case, the IC dissipates significant power, $P_D = V_{IN} \times I_{CLP}$, making thermal shutdown more likely.

Reverse Current Protection (RCP) "Ideal Diode"

In situations when V_{OUT} is driven above V_{IN} (for example when USB charging with elevated voltage at VBUS), the dynamic switch control turns OFF MOSFET B automatically due to its 60mV droop regulation control loop. MOSFET B's body diode points in the opposite direction of the current-limiting MOSFET A. The reverse blocking MOSFET B is inherently turned OFF whenever $V_{OUT} > V_{IN}$ - 60mV and turned ON again when $V_{OUT} < V_{IN}$ – 60mV.

Every time the device starts up, it prechecks if V_{OUT} is higher than V_{IN} or not. If yes, MOSFET B is kept OFF and reverse current is blocked. Then, after V_{OUT} returns below V_{IN}, MOSFET B is turned ON quickly within 50µs. The fast recovery of MOSFET B is assisted by the internal gate-drive charge pump, which is enabled whenever EN = 1, even during RCP (when MOSFET B is OFF). Since the gate-drive voltage is already present, a fast recovery time is easily achieved as soon as V_{OUT} falls below V_{IN} by 60mV.

Over Temperature Protection (OTP)

The KTS1690A features thermal shutdown to prevent the device from overheating. The internal MOSFETs turn OFF when the junction temperature exceeds +150°C (typ), and $\overline{FLT}$ is asserted. The device exits thermal shutdown after the junction temperature cools by 25°C (typ) hysteresis, and $\overline{FLT}$ is de-asserted.

Fault Reporting ($\overline{FLT}$)

In a current limit protection (CLP), over current protection (OCP), short-circuit protection (SCP), or over temperature protection (OTP) condition, the open-drain $\overline{FLT}$ pin is asserted LOW. A pull-up resistor should be connected from the $\overline{FLT}$ pin to the system I/O voltage rail. The $\overline{FLT}$ output returns to the high-Z state automatically once the fault condition is removed. The RCP circuit does not trigger a $\overline{FLT}$ indication.

For CLP events, an internal 8ms (typ) timer delays the fault indication at the $\overline{FLT}$ pin. However, for other fault events, the $\overline{FLT}$ indication asserts immediately. The $\overline{FLT}$ output flag is specifically designed to not toggle during a fault event, or when transitioning from a CLP fault to an OTP fault, or when recovering from an OTP fault and going back into a CLP fault. To prevent toggling, an internal 17ms (typ) timer delays the release of the $\overline{FLT}$ pin to the high-Z state after recovery from all faults.

Table 1. $\overline{FLT}$ Open-Drain Output Flag Truth Table

EN	FON	VIN	$\overline{FLT}$	Event or Condition
X	X	< V_{UVLO}	Z	UVLO, Switch Off
L	X	2.5V to 5.5V	Z	Shutdown Mode, Switch Off
H	L	2.5V to 5.5V	Z	Device Enabled, Soft-Start Slew-Rate Enabled
H	H	2.5V to 5.5V	Z	Device Enabled, Fast Turn ON Enabled
H	X	2.5V to 5.5V	L	Device Enabled, CLP Event, Switch is on
H	X	2.5V to 5.5V	L	Device Enabled, OCP or SCP or OTP Event, Switch Open
X	X	2.5V to 5.5V & V_{OUT} > V_{IN}	Z	RCP Event, Switch Open

Applications Information

C_{IN} Input Capacitor

For most applications, connect a 10µF or larger ceramic capacitor as close as possible to the device from IN to GND to minimize the effect of parasitic trace inductance. For USB fast role swap (FSR) applications that use the Fast Turn ON feature, connect a 47µF ceramic capacitor as close as possible to the device. Select a C_{IN} with voltage rating of 6.3V or higher. In most applications, the regulated 5V source that feeds IN will have additional bulk capacitance at its output. 57µF or more of additional bulk capacitance near the IN pin is typical.

C_{OUT} Output Capacitor

The internal soft-start function allows the KTS1690A to charge an output capacitor up to 100µF without turning OFF due to overcurrent. Typically, USB VBUS is 10µF nominal at the local side, but capability to 100µF allows for high capacitance in a remote device connected to the USB port. As a minimum, it is recommended to bypass OUT with a 1µF to 10uF ceramic capacitor and place it as close as possible to the OUT pin. Select a C_{OUT} with voltage rating of 50V or higher to survive ESD and surge events.

Cb Bias Capacitor

Competing pin-to-pin devices may require a 1nF Cb bias capacitor at the CAP pin. The KTS1690A allows this capacitor to maintain pin-to-pin functionality for dual-source PCB layouts. However, the KTS1690A does not use or require this capacitor. Therefore, the capacitor may be de-populated to save cost. In this case, the CAP pin is no connect (N.C.). The CAP pin is internally connected with metal to the GND pins. Therefore, the CAP pin may also be connected on the PCB to the GND pins and the PCB ground plane for slightly better thermal power dissipation.

Optional Schottky

Optionally connect an external Schottky diode from MID to OUT to improve transient performance for applications where the load steps from no-load to heavy load very quickly. When a load transient starts from a no-load condition, the RCP recovery time can take up to 15µs, and an external Schottky may reduce VOUT droop during this time. However, for load-transients where the minimum load is 10mA or higher, the RCP recovery is faster, and an external Schottky diode only provides minimal benefit.

Recommended PCB Layout

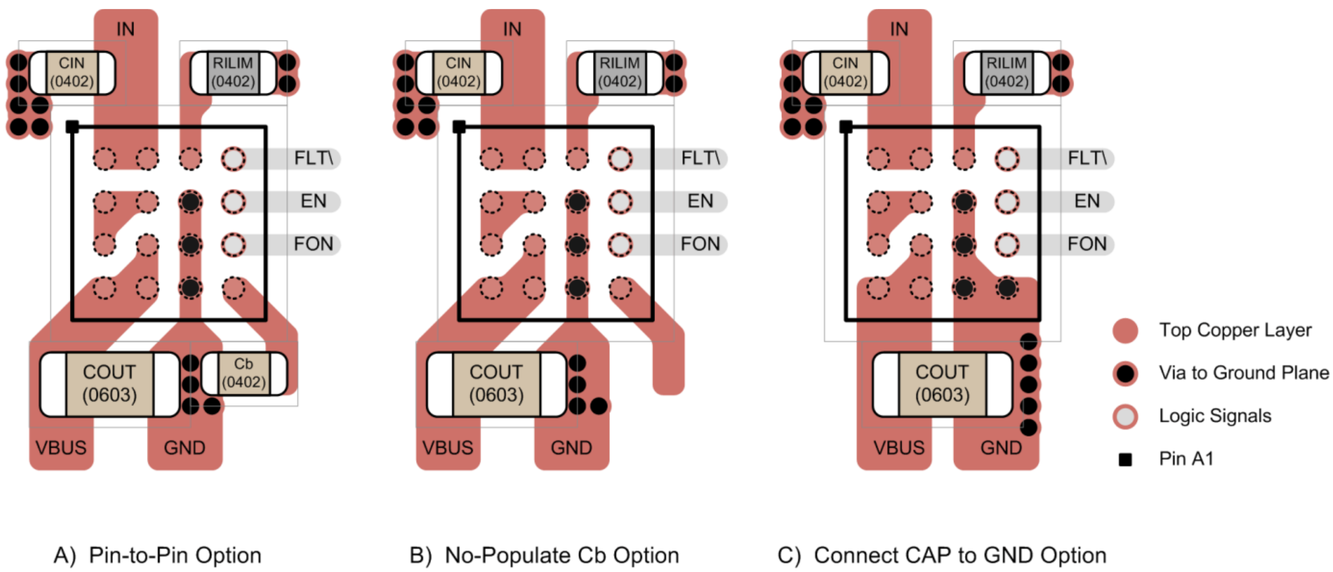


Figure 4. Recommended PCB Layout

Safe Operating Area (SOA)

See Figure 5 for the SOA of the KTS1690A. SOA curves are normally associated with discrete MOSFETs (which are sometimes co-package with a controller IC). In these competing systems, precautions are necessary to stay within the SOA area. However, the KTS1690A is a monolithic IC with some integrated protection features to *automatically* keep its operation within the SOA area (so long as the abs. max. rating AMR voltage is observed). For example, it includes settable current limit protection (CLP). It also includes over-temperature protection (OTP) that is measured on the same monolithic die as the integrated power MOSFETs. Additionally, soft-start is controlled with a voltage ramp and current limit protection (Soft-Start CLP) to safely soft-start even in applications with very high capacitance at the output. Furthermore, the integrated TVS and back-to-back MOSFET switch are optimized to work together as a system, including their tolerances over temperature and process corners.

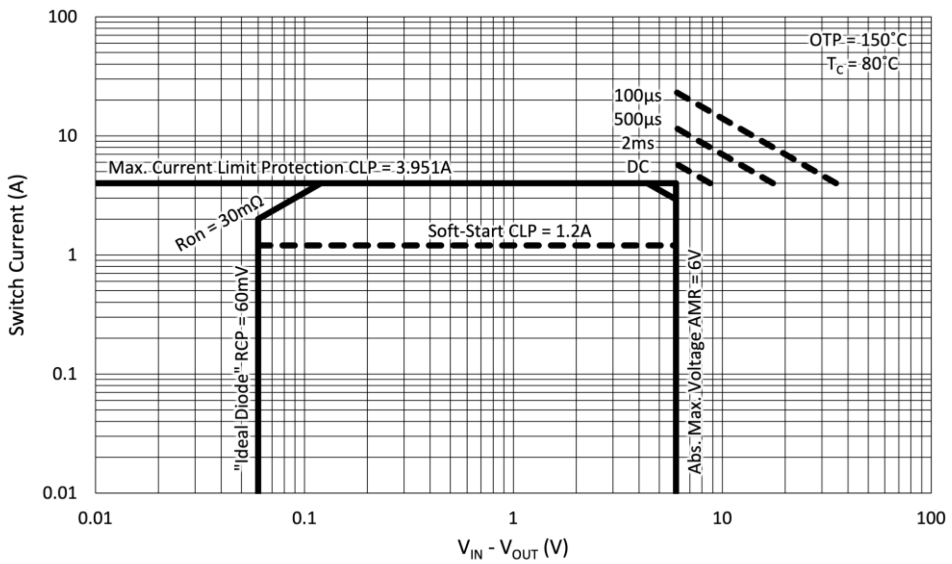
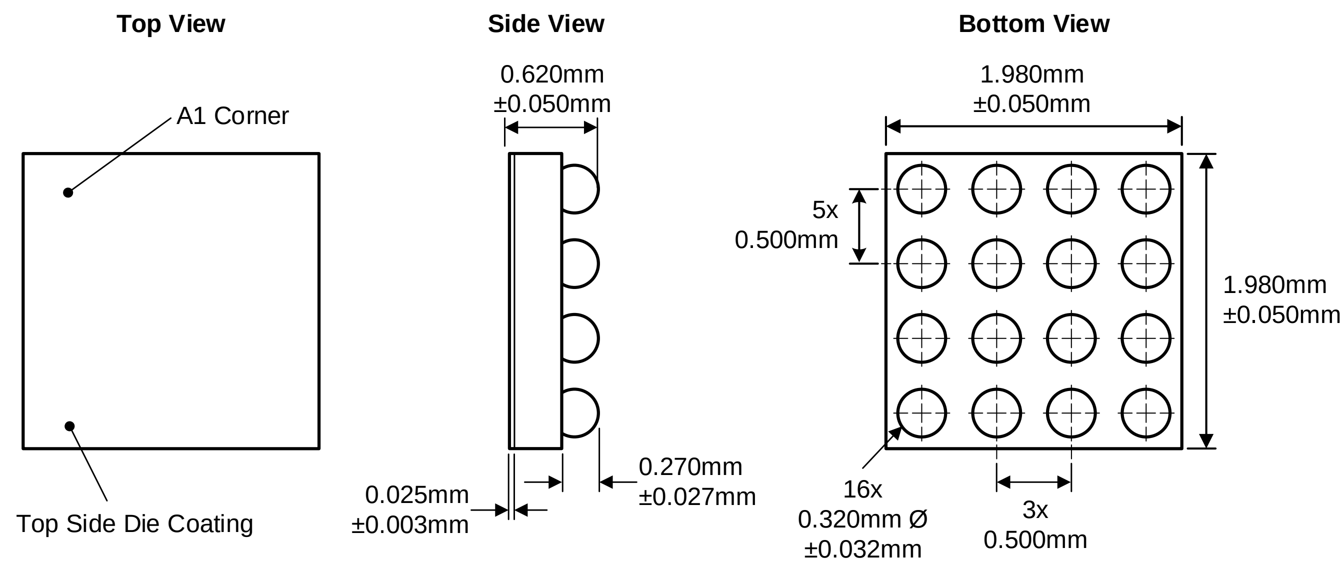


Figure 5. Safe Operating Area (SOA) for TC = 80℃

Packaging Information

WLCSP44-16 (1.980mm x 1.980mm x 0.620mm)



Recommended Footprint