2-Bit Dual-Supply Non-Inverting Level Translator

NLSV2T244

The NLSV2T244 is a 2−bit configurable dual−supply voltage level translator. The input A_n and output B_n ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low−voltage translation from the input A_n to the output B_n port.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- High−Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non−preferential V_{CCA} and V_{CCB} Sequencing
- Outputs at 3−State until Active V_{CC} is Reached
- Power−Off Protection
- Outputs Switch to 3−State with V_{CCB} at GND
- Small Packaging: UDFN8, SO−8, Micro8
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

- ESD Protection for All Pins:
   HBM (Human Body Model) > 5000 V

MARKING DIAGRAMS

UDFN8
MU SUFFIX
CASE 517AJ

UPM

UP = Specific Device Code
M = Date Code
■ = Pb−Free Package
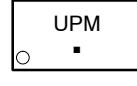
SO−8
D SUFFIX
CASE 751
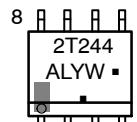
2T244
ALYW ■

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb−Free Package
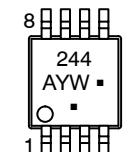
Micro8
DM SUFFIX
CASE 846A

244
AYW ■

A = Assembly Location
Y = Year
W = Work Week
■ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NLSV2T244MUTAG	UDFN8 (Pb−Free)	3000 / Tape & Reel
NLSV2T244DR2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NLSV2T244DMR2G	Micro8 (Pb−Free)	4000 / Tape & Reel
NLVSV2T244DMR2G*	Micro8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NLSV2T244
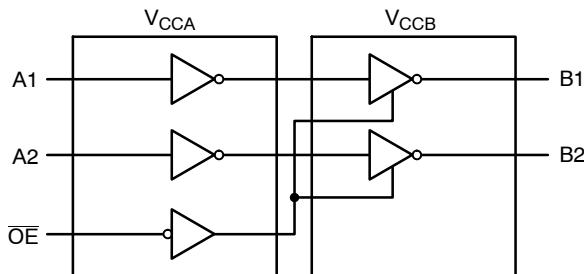
Figure 1. Logic Diagram

PIN ASSIGNMENTS

UDFN8
(Top View)

SOIC−8
(Top View)

Micro8
(Top View)
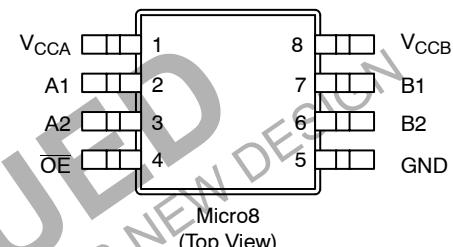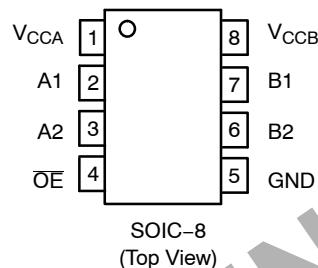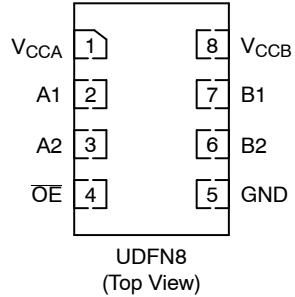
PIN ASSIGNMENT

PIN	FUNCTION
V$_{CCA}$	Input Port DC Power Supply
V$_{CCB}$	Output Port DC Power Supply
GND	Ground
A$_n$	Input Port
B$_n$	Output Port
$\overline{OE}$	Output Enable

TRUTH TABLE

Inputs		Outputs
$\overline{OE}$	A$_n$	B$_n$
L	L	L
L	H	H
H	X	3−State

MAXIMUM RATINGS

Symbol	Rating		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		−0.5 to +5.5		V
V_I	DC Input Voltage	A_n	−0.5 to +5.5		V
V_C	Control Input	$\overline{OE}$	−0.5 to +5.5		V
V_O	DC Output Voltage (Power Down)	B_n	−0.5 to +5.5	$V_{CCA} = V_{CCB} = 0$	V
	(Active Mode)	B_n	−0.5 to +5.5		V
	(Tri−State Mode)	B_n	−0.5 to +5.5		V
I_{IK}	DC Input Diode Current		−20	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current		−50	$V_O <$ GND	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CCA}, I_{CCB}	DC Supply Current Per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature		−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage		0.9	4.5	V
V_I	Bus Input Voltage		GND	4.5	V
V_C	Control Input	$\overline{OE}$	GND	4.5	V
V_{IO}	Bus Output Voltage (Power Down Mode)	B_n	GND	4.5	V
	(Active Mode)	B_n	GND	V_{CCB}	V
	(Tri−State Mode)	B_n	GND	4.5	V
T_A	Operating Temperature Range		−40	+85	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate V_I, from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ±0.3 V		0	10	nS

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V$_{CCA}$ (V)	V$_{CCB}$ (V)	−40°C to +85°C		Unit
					Min	Max	
V$_{IH}$	Input HIGH Voltage (An, $\overline{OE}$)		3.6 − 4.5	0.9 − 4.5	2.2	–	V
			2.7 − 3.6		2.0	–	
			2.3 − 2.7		1.6	–	
			1.4 − 2.3		0.65 * V$_{CCA}$	–	
			0.9 − 1.4		0.9 * V$_{CCA}$	–	
V$_{IL}$	Input LOW Voltage (An, $\overline{OE}$)		3.6 − 4.5	0.9 − 4.5	–	0.8	V
			2.7 − 3.6		–	0.8	
			2.3 − 2.7		–	0.7	
			1.4 − 2.3		–	0.35 * V$_{CCA}$	
			0.9 − 1.4		–	0.1 * V$_{CCA}$	
V$_{OH}$	Output HIGH Voltage	I$_{OH}$ = −100 µA; V$_I$ = V$_{IH}$	0.9 − 4.5	0.9 − 4.5	V$_{CCB}$ − 0.2	–	V
		I$_{OH}$ = −0.5 mA; V$_I$ = V$_{IH}$	0.9	0.9	0.75 * V$_{CCB}$	–	
		I$_{OH}$ = −2 mA; V$_I$ = V$_{IH}$	1.4	1.4	1.05	–	
		I$_{OH}$ = −6 mA; V$_I$ = V$_{IH}$	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I$_{OH}$ = −12 mA; V$_I$ = V$_{IH}$	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I$_{OH}$ = −18 mA; V$_I$ = V$_{IH}$	2.3	2.3	1.7	–	
			3.0	3.0	2.4	–	
		I$_{OH}$ = −24 mA; V$_I$ = V$_{IH}$	3.0	3.0	2.2	–	
V$_{OL}$	Output LOW Voltage	I$_{OL}$ = 100 µA; V$_I$ = V$_{IL}$	0.9 − 4.5	0.9 − 4.5	–	0.2	V
		I$_{OL}$ = 0.5 mA; V$_I$ = V$_{IL}$	1.1	1.1	–	0.3	
		I$_{OL}$ = 2 mA; V$_I$ = V$_{IL}$	1.4	1.4	–	0.35	
		I$_{OL}$ = 6 mA; V$_I$ = V$_{IL}$	1.65	1.65	–	0.3	
		I$_{OL}$ = 12 mA; V$_I$ = V$_{IL}$	2.3	2.3	–	0.4	
			2.7	2.7	–	0.4	
		I$_{OL}$ = 18 mA; V$_I$ = V$_{IL}$	2.3	2.3	–	0.6	
			3.0	3.0	–	0.4	
		I$_{OL}$ = 24 mA; V$_I$ = V$_{IL}$	3.0	3.0	–	0.55	
I$_I$	Input Leakage Current	V$_I$ = V$_{CCA}$ or GND	0.9 − 4.5	0.9 − 4.5	−1.0	1.0	µA
I$_{OFF}$	Power−Off Leakage Current	$\overline{OE}$ = 0 V	0 0.9 − 4.5	0.9 − 4.5 0	−1.0 −1.0	1.0 1.0	µA
I$_{CCA}$	Quiescent Supply Current	V$_I$ = V$_{CCA}$ or GND; I$_O$ = 0, V$_{CCA}$ = V$_{CCB}$	0.9 − 4.5	0.9 − 4.5	–	1.0	µA
I$_{CCB}$	Quiescent Supply Current	V$_I$ = V$_{CCA}$ or GND; I$_O$ = 0, V$_{CCA}$ = V$_{CCB}$	0.9 − 4.5	0.9 − 4.5	–	1.0	µA
I$_{CCA}$ + I$_{CCB}$	Quiescent Supply Current	V$_I$ = V$_{CCA}$ or GND; I$_O$ = 0, V$_{CCA}$ = V$_{CCB}$	0.9 − 4.5	0.9 − 4.5	–	2.0	µA
ΔI$_{CCA}$	Increase in I$_{CC}$ per Input Voltage, Other Inputs at V$_{CCA}$ or GND	V$_I$ = V$_{CCA}$ − 0.6 V; V$_I$ = V$_{CCA}$ or GND	4.5 3.6	4.5 3.6	–	10 5.0	µA
ΔI$_{CCB}$	Increase in I$_{CC}$ per Input Voltage, Other Inputs at V$_{CCA}$ or GND	V$_I$ = V$_{CCA}$ − 0.6 V; V$_I$ = V$_{CCA}$ or GND	4.5 3.6	4.5 3.6	–	10 5.0	µA
I$_{OZ}$	I/O Tri−State Output Leakage Current	T$_A$ = 25°C, $\overline{OE}$ = 0 V	0.9 − 4.5	0.9 − 4.5	−1.0	1.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TOTAL STATIC POWER CONSUMPTION ($I_{CCA} + I_{CCB}$)

V_{CCA} (V)	−40°C to +85°C										Unit
	V_{CCB} (V)										
	4.5		3.3		2.8		1.8		0.9		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
4.5		2		2		2		2		< 1.5	µA
3.3		2		2		2		2		< 1.5	µA
2.8		< 2		< 1		< 1		< 0.5		< 0.5	µA
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	µA
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	µA

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power−up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CCA} (V)	−40°C to +85°C										Unit
			V_{CCB} (V)										
			4.5		3.3		2.8		1.8		1.2		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL} (Note 1)	Propagation Delay, A_n to B_n	4.5		1.6		1.8		2.0		2.1		2.3	nS
		3.3		1.7		1.9		2.1		2.3		2.6	
		2.8		1.9		2.1		2.3		2.5		2.8	
		1.8		2.1		2.4		2.5		2.7		3.0	
		1.2		2.4		2.7		2.8		3.0		3.3	
t_{PZH}, t_{PZL} (Note 1)	Output Enable, $\overline{OE}$ to B_n	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{PHZ}, t_{PLZ} (Note 1)	Output Disable, $\overline{OE}$ to B_n	4.5		2.6		3.8		4.0		4.1		4.3	nS
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{OSHL}, t_{OSLH} (Note 1)	Output to Output Skew, Time	4.5		0.15		0.15		0.15		0.15		0.15	nS
		3.3		0.15		0.15		0.15		0.15		0.15	
		2.5		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

1. Propagation delays defined per Figure 2.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
C_{IN}	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or V_{CCA}, f = 10 MHz	20	pF

2. Typical values are at $T_A = +25°C$.
3. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:
$I_{CC(operating)} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

NLSV2T244
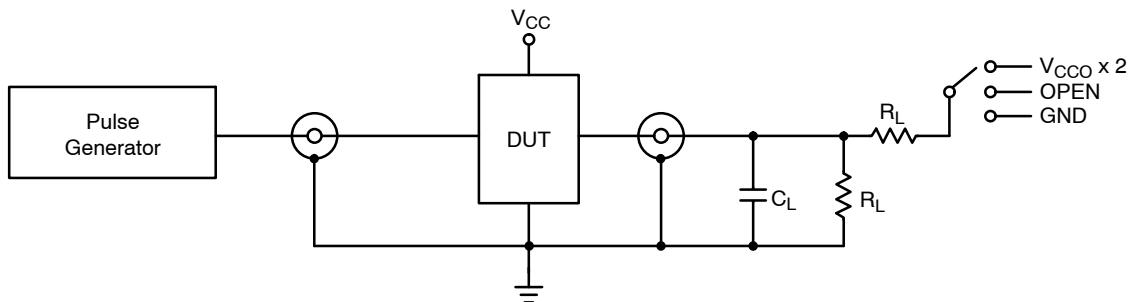
Figure 2. AC (Propagation Delay) Test Circuit

Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	V_{CCO} x 2
t_{PHZ}, t_{PZH}	GND

C_L = 15 pF or equivalent (includes probe and jig capacitance)
R_L = 2 kΩ or equivalent
Z_{OUT} of pulse generator = 50 Ω
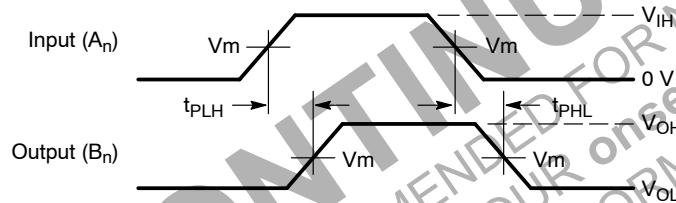
**Waveform 1 – Propagation Delays**
$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns
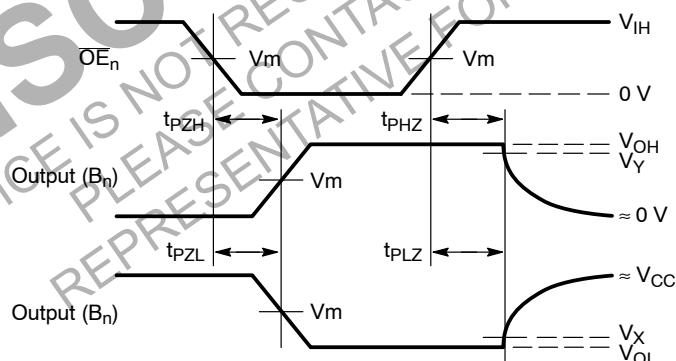
Waveform 2 – Output Enable and Disable Times
$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 3. AC (Propagation Delay) Test Circuit Waveforms

Symbol	V_{CC}				
	3.0 V – 4.5 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	0.9 V – 1.3 V
V_{mA}	V_{CCA}/2	V_{CCA}/2	V_{CCA}/2	V_{CCA}/2	V_{CCA}/2
V_{mB}	V_{CCB}/2	V_{CCB}/2	V_{CCB}/2	V_{CCB}/2	V_{CCB}/2
V_X	V_{OL} x 0.1	V_{OL} x 0.1	V_{OL} x 0.1	V_{OL} x 0.1	V_{OL} x 0.1
V_Y	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9

onsemi

UDFN8 1.8x1.2, 0.4P
CASE 517AJ
ISSUE O

DATE 08 NOV 2006

8

1

SCALE 4:1

TOP VIEW

| 0.10 | C |

| 0.10 | C |

D ▸ A B

PIN ONE
REFERENCE

E

DETAIL A
NOTE 5

L1

SIDE VIEW

| 0.05 | C |

| 0.05 | C |

(A3)

A

A1

C **SEATING PLANE**

BOTTOM VIEW

e/2

e

(b2)

(L2)

DETAIL A

8X L

1   4

8   5

8X b

| ⊕ | 0.10 Ⓜ | C | A | B |
| | 0.05 Ⓜ | C | NOTE 3 |

MOUNTING FOOTPRINT
SOLDERMASK DEFINED

7X
0.22

8X
0.66

1.50

1

0.32

0.40 PITCH

DIMENSIONS: MILLIMETERS
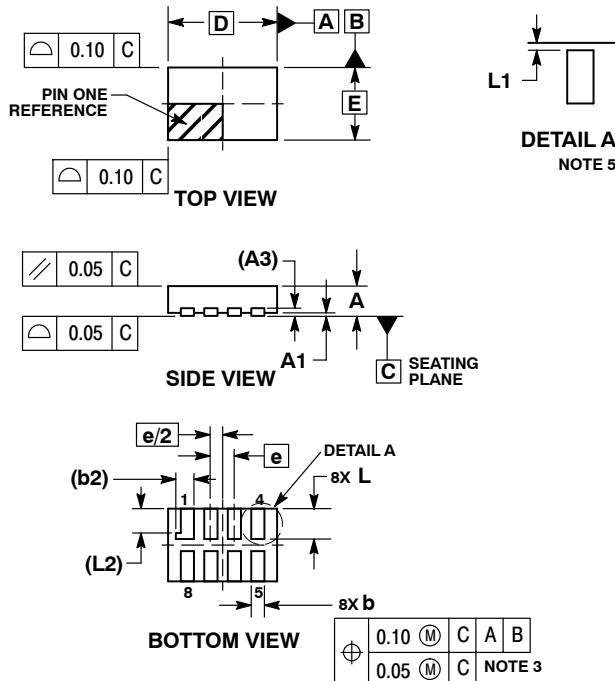
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
b2	0.30 REF	
D	1.80 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.45	0.55
L1	0.00	0.03
L2	0.40 REF	

GENERIC
MARKING DIAGRAM*

XXM
●

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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DESCRIPTION:	UDFN8 1.8X1.2, 0.4P		**PAGE 1 OF 1**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

8
1
SCALE 1:1
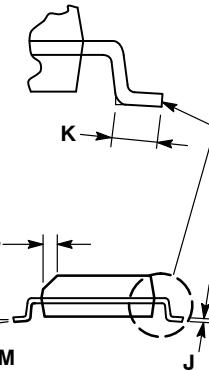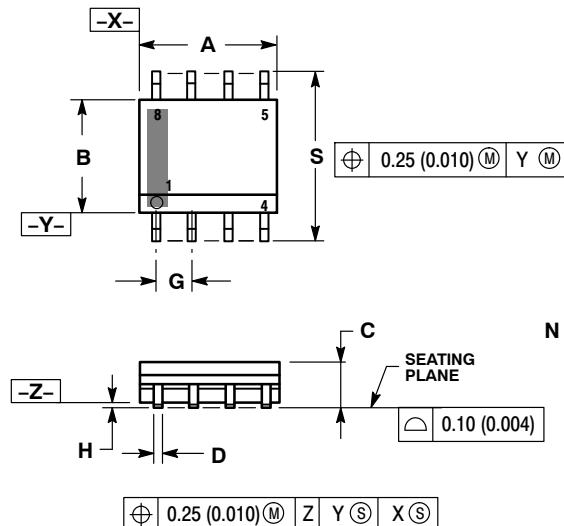
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

$\oplus$ | 0.25 (0.010) Ⓜ | Y Ⓜ

$\oplus$ | 0.10 (0.004)

$\oplus$ | 0.25 (0.010) Ⓜ | Z Y Ⓢ X Ⓢ

N X 45°

SEATING PLANE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244
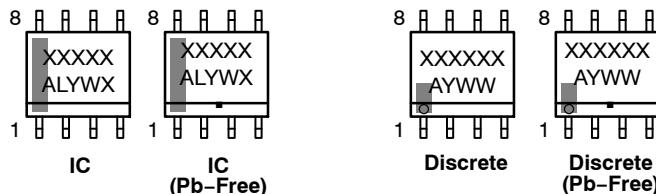
SOLDERING FOOTPRINT*

$\frac{1.52}{0.060}$

$\frac{7.0}{0.275}$

$\frac{4.0}{0.155}$

$\frac{0.6}{0.024}$

$\frac{1.270}{0.050}$

SCALE 6:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

8 XXXXX ALYWX — IC

8 XXXXX ALYWX — IC (Pb−Free)

8 XXXXXX AYWW — Discrete

8 XXXXXX AYWW — Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−8 NB		PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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Micro8
CASE 846A−02
ISSUE K

SCALE 2:1

DATE 16 JUL 2020

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.

2. CONTROLLING DIMENSION: MILLIMETERS

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.

4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.

5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.

6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

TOP VIEW

NOTE 3

DETAIL A

END VIEW

SIDE VIEW

**GENERIC
MARKING DIAGRAM***
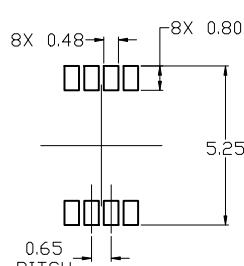
RECOMMENDED
MOUNTING FOOTPRINT

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

■ For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

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