TEXAS INSTRUMENTS

OPA4323, OPA323, OPA2323
SBOSAE8A – OCTOBER 2023 – REVISED NOVEMBER 2023

OPAx323 20 MHz High Bandwidth, 100 dB CMRR, Low Voltage (1.7 V to 5.5 V), RRIO Zero-Cross Operational Amplifier

1 Features

- Zero cross amplifier for 1.7 V to 5.5 V applications
- High gain-bandwidth product: 20 MHz
- Fast slew-rate: 33 V/µs typical
- Fast 0.01% settling: 200 ns typical for 2 V step
- Low input offset voltage: ±150 µV typical
- Low noise floor: 5.5 nV/√Hz typical at 10 kHz
- High output current: ±110 mA typical I_{SC} at 5.5 V
- Quiescent current: 1.6 mA/ch typical
- Rail-to-rail input and output
- Unity-gain stable
- Drives up to 150 pF without sustained oscillations
- Internal RFI and EMI filtered input pins
- Operating temperature range: –40°C to 125°C

2 Applications

- Amplifier driver for ADCs
- High side current sensing
- Motor rotary encoders
- Transimpedance photodiode amplifiers
- Audio microphone pre-amplifiers
- Ultrasonic transducers

3 Description

The OPAx323 family of op amps includes single (OPA323), dual (OPA2323), and quad-channel (OPA4323), low-voltage (1.7 V to 5.5 V), high-bandwidth (20 MHz) amplifiers (op amps) with a zero-crossover input stage and a rail-to-rail output stage. The zero-crossover input stage enables OPAx323 to achieve high linearity and low distortion for input signals with rail-to-rail swing that are typical in ADC driver applications. Gain-bandwidth of 20 MHz provides a fast settling response for ADC sampling speeds between 0.5 to 5 MSPS depending on the settling performance required. OPAx323 is well-optimized for power savings as it consumes just 1.6 mA typical quiescent current.

OPAx323 easily supports precision performance in high gain voltage sensing applications such as the wheatsone bridge, as it features maximum offset drift of 2 µV/°C and thermal noise floor of 5.5 nV/rt-Hz with a minimum of 100 dB CMRR. This unique combination of higher precision (low offset, drift, noise, distortion, and CMRR) and higher gain-bandwidth (fast settling and slewing) enables use in multiple applications such as the motor rotary encoders, microphone audio preamplfiers and ultrasonic transducers.

OPAx323 achieves a high slew-rate of 33 V/µs allowing for fast detection of faults in motor current sensing applications. Unlike traditional amplifiers, the zero-cross over input stage allows for identical precision performance for both low and high-side sensing applications, thus making OPAx323 the best choice for current sensing in a variety of end equipments such as the solar string inverters, power delivery, grid and EV infrastructure. OPAx323S devices provide shutdown functionality for additional power savings and help disable the amplifier when idle. The family features standard and small size as well as leaded and QFN packages across all the channel variants.

Device Information

PART NUMBER[1]	CHANNEL COUNT	PACKAGE[4]	PACKAGE SIZE[5]
OPA323	Single	DBV (SOT-23, 5) [3]	2.9 mm × 2.8 mm
		DCK (SC70, 5)	2 mm × 1.25 mm
		DRL (SOT-5X3, 5) [3]	1.6 mm × 1.6 mm
OPA323S [2]	Single, Shutdown	DBV (SOT-23, 6) [3]	2.9 mm × 2.8 mm
		DCK (SC70, 6) [3]	2 mm × 1.25 mm
OPA2323	Dual	D (SOIC, 8)	4.9 mm × 6 mm
		DDF (SOT-23, 8)[3]	2.9 mm × 2.8 mm
		DSG (WSON, 8) [3]	2 mm × 2 mm
		DGK (VSSOP, 8) [3]	3 mm × 4.9 mm
		PW (TSSOP, 8)[3]	3 mm × 6.4 mm
OPA2323S [2]	Dual, Shutdown	RUG (X2QFN, 10) [3]	1.5 mm × 2 mm
OPA4323	Quad	D (SOIC, 14) [3]	8.65 mm × 6 mm
		PW (TSSOP, 14)	5 mm × 6.4 mm
		RUC (X2QFN, 14)[3]	2 mm × 2 mm
OPA4323S [2]	Quad, Shutdown	RTE (WQFN, 16) [3]	3 mm × 3 mm
		DYY (SOT-23, 16) [3]	4.2 mm × 2 mm

(1) See Section 4.
(2) Part number is for preview only.
(3) Package is for preview only.
(4) For more information, see Section 11.
(5) The package size (length × width) is a nominal value and includes pins, where applicable.
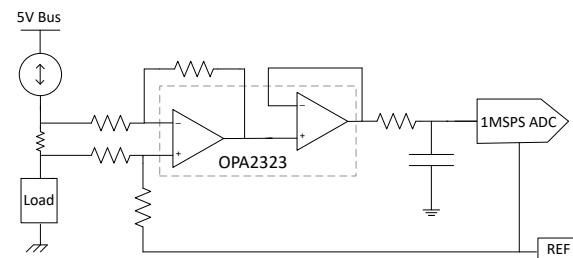
Bi-Directional, High-Side Current Sense Amplifier and ADC Driver

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4 Device Comparison Table

DEVICE	NO. OF CHANNELS	SHDN	PACKAGE LEADS										
			SC70 DCK	SOIC D	SOT-23 DBV[2]	SOT-23 DDF[2]	SOT-553 DRL[2]	SOT-23 DYY[2]	TSSOP PW	VSSOP DGK [2]	WQFN RTE	WSON DSG[2]	X2QFN RUG[2]
OPA323	1	NO	5	—	5	—	5	—	—	—	—	—	—
OPA323S[1]	1	YES	6	—	6	—	—	—	—	—	—	—	—
OPA2323	2	NO	—	8	—	8	—	—	8	8	—	8	—
OPA2323S[1]	2	YES	—	—	—	—	—	—	—	—	—	—	10
OPA4323	4	NO	—	14	—	—	—	—	14	—	—	—	—
OPA4323S	4	YES	—	—	—	—	—	16	—	—	16	—	—

(1) Devices are preview only.
(2) Packages are preview only.

Product Folder Links: *OPA4323 OPA323 OPA2323*

5 Pin Configuration and Functions
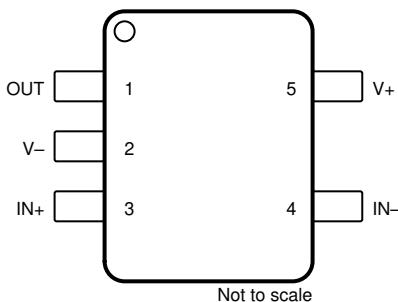
**Figure 5-1. OPA323 DBV Package,
5-Pin SOT-23
(Top View)**
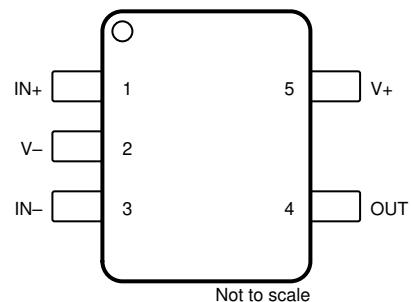
**Figure 5-2. OPA323 DCK and DRL Package,
5-Pin SC70 and 5-Pin SOT-5X3
(Top View)**

Table 5-1. Pin Functions: OPA323

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23	SC70, SOT-5X3		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	I	Positive (high) supply

(1)   I = input, O = output
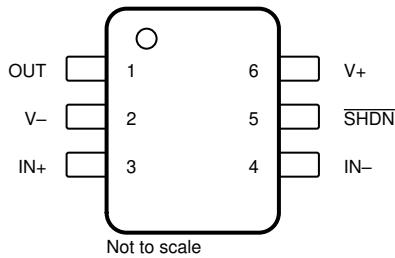
**Figure 5-3. OPA323S DBV Package,
6-Pin SOT-23
(Top View)**
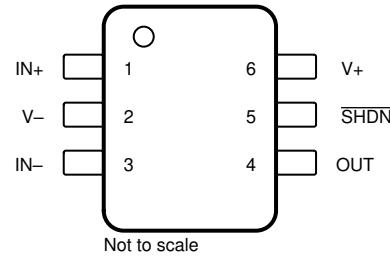
**Figure 5-4. OPA323S DCK Package,
6-Pin SC70
(Top View)**

Table 5-2. Pin Functions: OPA323S

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
$\overline{\text{SHDN}}$	5	5	I	Shutdown: low = amp disabled, high = amp enabled See *Shutdown Function* for more information
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply

(1) I = input, O = output

Product Folder Links: *OPA4323 OPA323 OPA2323*
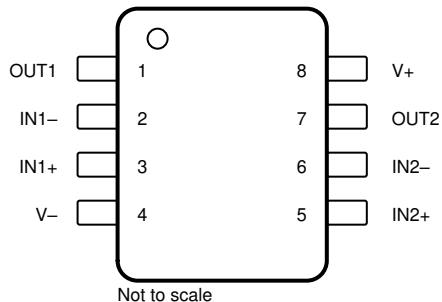
**Figure 5-5. OPA2323 D, PW, DGK, and DDF Package,
SOIC, TSSOP, VSSOP, and SOT-23-THIN
(Top View)**
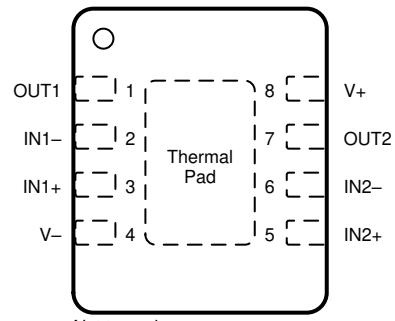
Connect exposed thermal pad to V–. For more information, see *Packages with an Exposed Thermal Pad*.

**Figure 5-6. OPA2323 DSG Package,
8-Pin WSON with Exposed Thermal Pad
(Top View)**

Table 5-3. Pin Functions: OPA2323

PIN		TYPE[1]	DESCRIPTION
NAME	SOIC, TSSOP, VSSOP, SOT-23-THIN, WSON		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

(1) I = input, O = output

Product Folder Links: *OPA4323 OPA323 OPA2323*
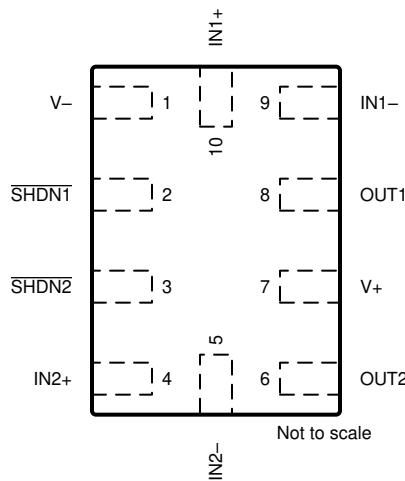
Figure 5-7. OPA2323S RUG Package
10-Pin X2QFN
(Top View)

Table 5-4. Pin Functions: OPA2323S

PIN		TYPE[1]	DESCRIPTION
NAME	X2QFN		
IN1–	9	I	Inverting input, channel 1
IN1+	10	I	Noninverting input, channel 1
IN2–	5	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	8	O	Output, channel 1
OUT2	6	O	Output, channel 2
$\overline{\text{SHDN1}}$	2	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. For more information, see *Shutdown Function*.
$\overline{\text{SHDN2}}$	3	I	Shutdown: low = amp disabled, high = amp enabled, channel 2. For more information, see *Shutdown Function*.
V–	1	I	Negative (low) supply or ground (for single-supply operation)
V+	7	I	Positive (high) supply

(1)   I = input, O = output

Product Folder Links: *OPA4323 OPA323 OPA2323*
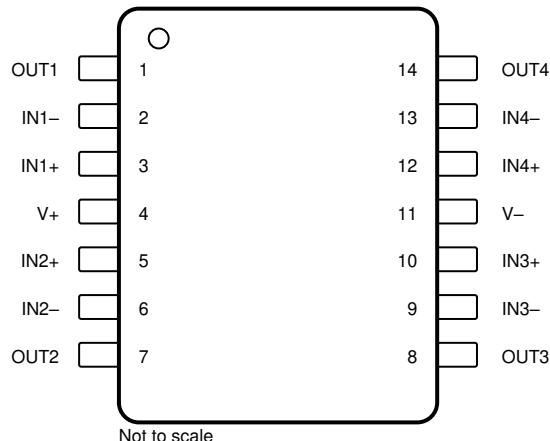
Figure 5-8. OPA4323 D and PW Package,
14-Pin SOIC and TSSOP
(Top View)

Table 5-5. Pin Functions: OPA4323

PIN		TYPE[1]	DESCRIPTION
NAME	SOIC, TSSOP		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

(1)   I = input, O = output

A.   Connect thermal pad to V–.

**Figure 5-9. OPA4323S RTE Package,
16-Pin WQFN With Exposed Thermal Pad
(Top View)**

Not to scale
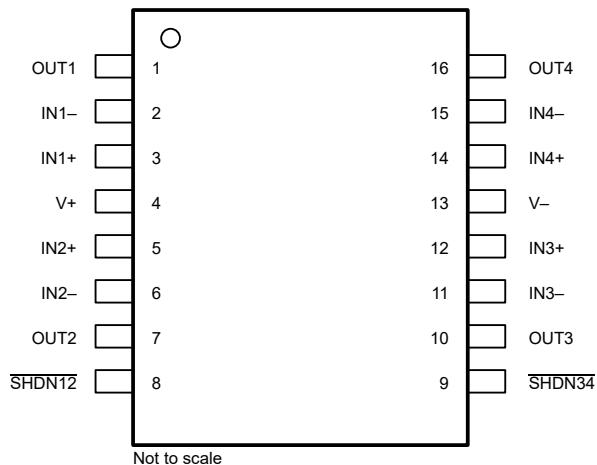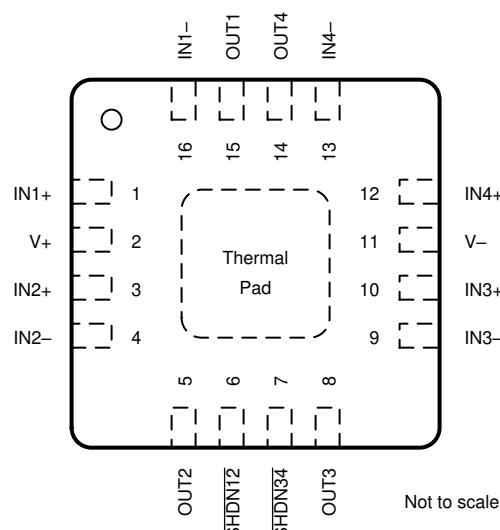
**Figure 5-10. OPA4323S DYY Package,
16-Pin SOT-23-THIN
(Top View)**

Table 5-6. Pin Functions: OPA4323S

PIN			TYPE[1]	DESCRIPTION
NAME	**WQFN**	**SOT-23-THIN**		
IN1+	1	3	I	Noninverting input, channel 1
IN1–	16	2	I	Inverting input, channel 1
IN2+	3	5	I	Noninverting input, channel 2
IN2–	4	6	I	Inverting input, channel 2
IN3+	10	12	I	Noninverting input, channel 3
IN3–	9	11	I	Inverting input, channel 3
IN4+	12	14	I	Noninverting input, channel 4
IN4–	13	15	I	Inverting input, channel 4
$\overline{\text{SHDN12}}$	6	8	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. For more information, see *Shutdown Function*.
$\overline{\text{SHDN34}}$	7	9	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. For more information, see *Shutdown Function*.
OUT1	15	1	O	Output, channel 1
OUT2	5	7	O	Output, channel 2
OUT3	8	10	O	Output, channel 3
OUT4	14	16	O	Output, channel 4
V–	11	13	I	Negative (low) supply or ground (for single-supply operation)
V+	2	4	I	Positive (high) supply

(1)   I = input, O = output

Product Folder Links: *OPA4323 OPA323 OPA2323*

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Supply voltage, V_S = (V+) – (V–)	0	7.0	V
Signal input pins	Common-mode voltage [2] [3]	– 0.5	6.0	V
	Differential voltage [2] [3]		±6.0	V
	Current [3]	–10	10	mA
Output short-circuit [4]		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1)   Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2)   Input pins can swing beyond (V+) as long as they stay with in 6.0 V. No diode structure from input pins to (V+).
(3)   Input pins are diode-clamped to (V–). Input signals that 0.3 V below (V–) must be current-limited to 10 mA or less.
(4)   Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]		±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	OPA4323	±500	V
			OPA323, OPA2323	±250	V

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.7	5.5	V
C_{BYP}	Bypass capacitor on the power supply pins [1]	0.1		µF
T_A	Specified temperature	–40	125	°C

(1)   For C_{BYP}, use low-ESR ceramic capacitors between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Ensure that C_{BYP} is placed as close to the device as possible and the supply trace routes through C_{BYP} before reaching the supply pin.

Product Folder Links: *OPA4323 OPA323 OPA2323*

6.4 Thermal Information for Single Channel

THERMAL METRIC [1]		OPA323			OPA323S		UNIT
		DBV [2] (SOT-23)	DCK (SC70)	DRL [2] (SOT-5X3)	DBV [2] (SOT-23)	DCK [2] (SC70)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.3	196.7	TBD	168.8	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.9	104.5	TBD	87.8	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	44.8	TBD	49.3	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.7	18.7	TBD	25.6	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.5	44.5	TBD	49.0	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	TBD	n/a	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview.

6.5 Thermal Information for Dual Channel

THERMAL METRIC [1]		OPA2323					OPA2323S	UNIT
		D (SOIC)	PW [2] (TSSOP)	DGK [2] (VSSOP)	DDF [2] (SOT-23-8)	DSG [2] (WSON)	RUG [2] (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.0	TBD	TBD	149.6	TBD	144.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.2	TBD	TBD	72.9	TBD	47.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.4	TBD	TBD	68.4	TBD	76.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.3	TBD	TBD	4.0	TBD	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.6	TBD	TBD	68.1	TBD	75.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	TBD	TBD	n/a	TBD	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview.

6.6 Thermal Information for Quad Channel

THERMAL METRIC [1]		OPA4323		OPA4323S		UNIT
		D [2] (SOIC)	PW (TSSOP)	DYY [2] (SOT)	RTE [2] (WQFN)	
		14 PINS	14 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	115.8	113.7	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	44.9	49.1	52.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	58.7	42.4	23.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	5.2	1.6	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	58.1	42.2	23.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	n/a	n/a	8.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview.

Product Folder Links: *OPA4323 OPA323 OPA2323*

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.85 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 1.8 V to 5.5 V			±0.15	±1.25	mV
		V_S = 1.8 V to 5.5 V	T_A = –40°C to 125°C			±1.35	
dV_{OS}/dT	Input offset voltage drift [1]	V_S = 1.8 V to 5.5 V	T_A = –40°C to 125°C		±0.4	±1.8	µV/°C
PSRR	Input offset voltage versus power supply	V_S = 1.8 V to 5.5 V			±5	±20	µV/V
	Channel separation	f = 10 kHz			±1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current [1]	V_S = 1.8 V and V_S = 5 V			±0.5	±20	pA
		V_S = 1.8 V and V_S = 5 V	T_A = –40°C to 125°C			±1600	pA
I_{OS}	Input offset current [1]	V_S = 1.8 V and V_S = 5 V			±0.25		pA
		V_S = 1.8 V and V_S = 5 V	T_A = –40°C to 125°C			±120	pA
NOISE							
E_N	Input voltage noise	f = 0.1 to 10 Hz			2.8		µV$_{PP}$
e_N	Input voltage noise density	f = 100 Hz			24		nV/√Hz
		f = 1 kHz			9		
		f = 10 kHz			5.5		
i_N	Input current noise [2]	f = 1 kHz			20		fA/√Hz
INPUT VOLTAGE RANGE							
V_I	Input voltage range	V_S = 1.8 V to 5.5 V		(V–) – 0.2		(V+) + 0.15	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.2 V ≤ V_{CM} ≤ (V+) + 0.10 V		100	114		dB
		V_S = 5.5 V, (V–) – 0.2 V ≤ V_{CM} ≤ (V+) + 0.15 V		90	104		dB
		V_S = 5.5 V, (V–) – 0.2 V ≤ V_{CM} ≤ (V+) + 0.15 V	T_A = –40°C to 125°C	84			dB
		V_S = 1.8 V, (V–) – 0.1 V ≤ V_{CM} ≤ (V+) + 0.05 V		85	103		dB
		V_S = 1.8 V, (V–) – 0.1 V ≤ V_{CM} ≤ (V+) + 0.05 V	T_A = –40°C to 125°C	80			dB
INPUT IMPEDANCE							
Z_{ID}	Differential				80 ‖ 2		GΩ ‖ pF
Z_{ICM}	Common-mode				100 ‖ 1		GΩ ‖ pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ to V_S / 2		103	120		dB
		V_S = 1.8 V, (V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ to V_S / 2		100	115		dB
		V_S = 5.5 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ to V_S / 2		112	125		dB
		V_S = 5.5 V, (V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ to V_S / 2 (OPA4310)		110	120		dB
		V_S = 5.5 V, (V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ to V_S / 2		108	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	V_S = 5.5 V, G = +1, R_L = 10kΩ, C_L = 100 pF	T_A = 25°C		20		MHz
SR	Slew rate	V_S = 5.5 V, G = +1, V_{STEP} = 5 V, R_L = 10kΩ, C_L = 100 pF			33		V/µs
THD+N	Total harmonic distortion + noise [3]	V_S = 5 V, G = +1, V_O = 4 V$_{P-P}$, f = 10 kHz, R_L = 600 Ω to V_S / 2, C_L = 50 pF			0.00125		%
t_S	Settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 10 pF			200		ns
		To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 10 pF			150		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 10 pF			250		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 10 pF			200		

Product Folder Links: *OPA4323 OPA323 OPA2323*

6.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.85 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GM	Gain Margin	V_S = 5.5 V, G = +1, R_L = 10 kΩ, C_L = 30 pF		15		dB
		V_S = 1.8 V, G = +1, R_L = 10 kΩ, C_L = 30 pF		15		dB
PM	Phase Margin	V_S = 5.5 V, G = +1, R_L = 10 kΩ, C_L = 30 pF		50		°
		V_S = 1.8 V, G = +1, R_L = 10 kΩ, C_L = 30 pF		52.5		°
$t_{overload}$	Overload recovery time	V_{IN} × gain > V_S		130		ns
EMIRR	Electro-magnetic interference rejection ratio	f = 1.8 GHz, V_{IN_EMIRR} = 100 mV		62		dB
OUTPUT						
V_o	Voltage output swing from rail	V_S = 1.8 V, R_L = 10 kΩ to V_S / 2		15	25	mV
		V_S = 5.5 V, R_L = 10 kΩ to V_S / 2		25	35	mV
		V_S = 5.5 V, R_L = 2 kΩ to V_S / 2		45	55	mV
I_{SC}	Short-circuit current [4]	V_S = 1.8 V	±20	±40		mA
		V_S = 5.5 V	±80	±110		mA
Z_O	Open-loop output impedance	f = 10 kHz		80		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 A		1.6	1.9	mA
		T_A = –40°C to 125°C			2.0	
	Power-on time	V_S = 0 to 5.5 V, 90% I_Q Level		25		µs
SHUTDOWN						
I_{QSD}	Shutdown current per amplifier [7]	All amplifiers disabled, $\overline{SHDN}$ = V–		0.5	1	µA
		All amplifiers disabled, $\overline{SHDN}$ = V–, T_A = –40 °C to 125 °C			1.5	µA
Z_{SHDN}	Output impedance during shutdown [7]	Amplifier disabled		43 || 11.5		GΩ || pF
V_{IH}	Logic high threshold voltage (amplifier enabled) [7]		(V–) + 1 V			V
V_{IL}	Logic low threshold voltage (amplifier disabled) [7]				(V–) + 0.2 V	V
t_{ON}	Amplifier enable time (full shutdown) [5] [6] [7]	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–		1		µs
	Amplifier enable time (partial shutdown) [5] [6] [7]	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–		1		
t_{OFF}	Amplifier disable time [5] [7]	G = +1, V_{CM} = V_S / 2, V_O = 0.1 × V_S / 2, R_L connected to V–		1		µs
	$\overline{SHDN}$ pin input bias current (per pin) [7]	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 1 V		50		nA
		(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.2 V		100		

(1)   Max / Min limit is specified based on characterization results.
(2)   Typical input current noise data to be specified based on design simulation results
(3)   Third-order filter; bandwidth = 80 kHz at –3 dB.

Product Folder Links: *OPA4323 OPA323 OPA2323*

(4)   Short circuit current specified here is average of sourcing and sinking short circuit currents

(5)   Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{\text{SHDN}}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

(6)   Full shutdown refers to the dual device having both channels 1 and 2 disabled ($\overline{\text{SHDN1}}$ = $\overline{\text{SHDN2}}$ = V–) and the quad device having all channels 1 to 4 disabled ($\overline{\text{SHDN12}}$ = $\overline{\text{SHDN34}}$ = V–). For partial shutdown, only one $\overline{\text{SHDN}}$ pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.

(7)   Shutdown section is on preview

6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

|		
V_S = 5.5 V	V_{CM} = V_S / 2	T_A = 25°C
No. of devices = 90	Mean = 1 pA	Sigma = 2 pA

Figure 6-1. Input Bias Current Distribution Histogram

V_S = 5.5 V	V_{CM} = V_S / 2	T_A = 85°C
No. of devices = 90	Mean = 13 pA	Sigma = 2 pA

**Figure 6-2. Input Bias Current Distribution Histogram**

V_S = 5.5 V	V_{CM} = V_S / 2	T_A = 25°C
No. of devices = 45	Mean = –0.1 pA	Sigma = 1.7 pA

Figure 6-3. Input Offset Current Distribution Histogram

V_S = 5.5 V	V_{CM} = V_S / 2	T_A = 85°C
No. of devices = 45	Mean = 1.1 pA	Sigma = 2.1 pA

Figure 6-4. Input Offset Current Distribution Histogram

No. of devices = 72

Figure 6-5. Input Offset Voltage vs Supply Voltage

Figure 6-6. Input Offset Voltage vs Supply Voltage

Product Folder Links: *OPA4323 OPA323 OPA2323*

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V− = −2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)
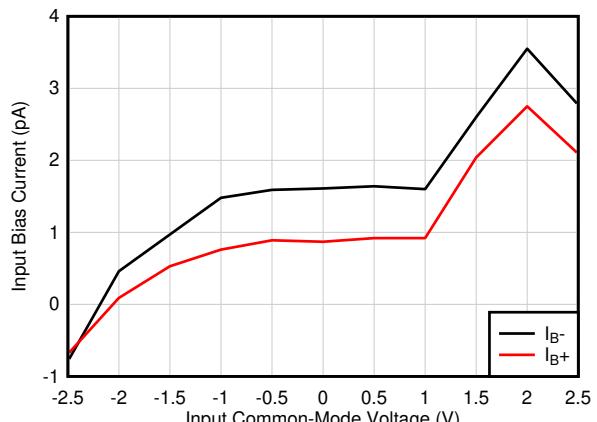
V+ = 2.5 V, V− = −2.5 V, V_{CM} = V_S/2

Figure 6-7. I_B vs Common-Mode Voltage

V+ = 2.5 V, V− = −2.5 V, V_{CM} = V_S/2
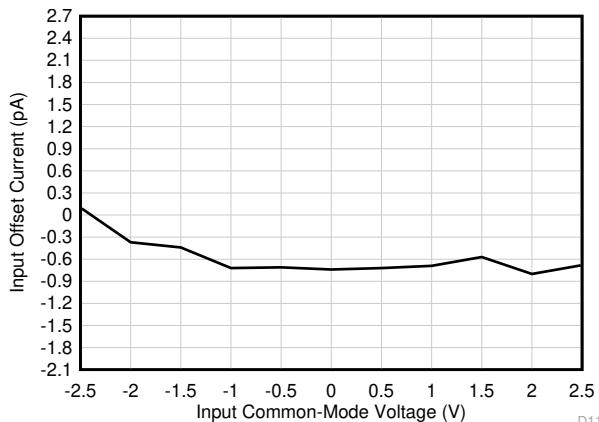
Figure 6-8. I_{OS} vs Common-Mode Voltage
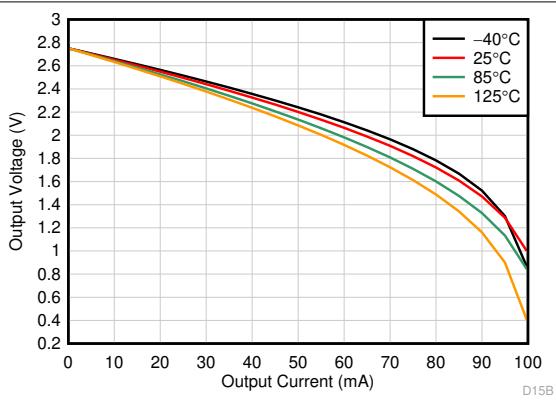
V+ = 2.75 V, V− = −2.75 V

Figure 6-9. Output Voltage Swing vs Output Current (Sourcing)
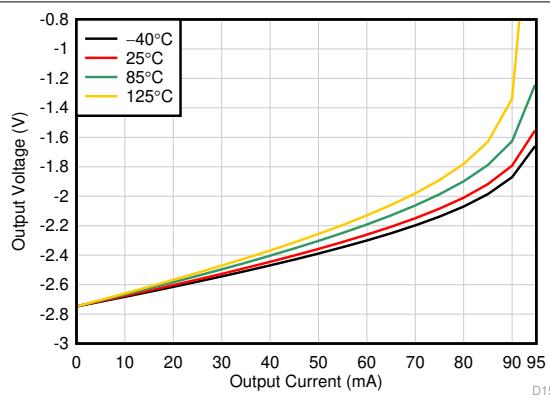
V+ = 2.75 V, V− = −2.75 V

Figure 6-10. Output Voltage Swing vs Output Current (Sinking)
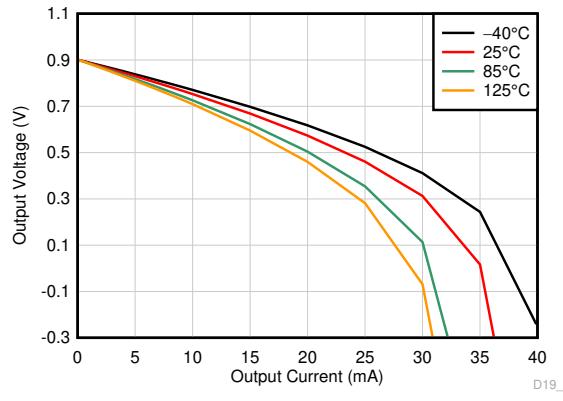
V+ = 0.9 V, V− = −0.9 V

Figure 6-11. Output Voltage Swing vs Output Current (Sourcing)
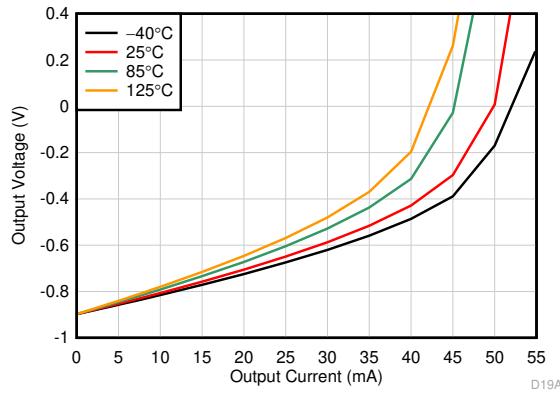
V+ = 0.9 V, V− = −0.9 V

Figure 6-12. Output Voltage Swing vs Output Current (Sinking)

Product Folder Links: *OPA4323 OPA323 OPA2323*

7 Detailed Description

7.1 Overview

The OPAx323 family of op amps includes single / dual / quad channel (OPA323, OPA2323, OPA4323), ultra low-voltage (1.7 V to 5.5 V), high-bandwidth (20 MHz) amplifiers. This family of amplifiers feature a zero-crossover input stage and a rail-to-rail output stage that can be used for variety of applications across industrial and automotive markets. The input common-mode voltage range includes signal swing beyond the supply rails, and allows the OPAx323 to be used in many single-supply or dual supply configurations. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications with the class AB output stage capable of driving smaller resistive loads.

OPAx323 family of zero-cross input stage amplifiers achieve high linearity for input signals with rail-to-rail swing that are typical in ADC driver applications in comparison to the complementary input stage amplifiers. Gain-bandwidth of 20 MHz helps provide a fast settling response for ADC sampling speeds between 0.5 to 5 MSPS depending on the settling performance required. OPAx323 easily supports precision performance in high gain voltage sensing applications (such as the wheatsone bridge), as it features maximum offset of 1.25 mV and drift of 1.8 µV/°C. This unique combination of high precision and high gain-bandwidth enables use in multiple applications such as the motor rotary encoders, microphone audio preamplfiers and ultrasonic transducers.

OPAx323 family consumes only 1.6 mA supply current per channel for 20 MHz gain bandwidth, thus providing a good AC performance at a very low power consumption. These devices achieve a high slew-rate of 33 V/µs allowing for fast detection of faults in motor current sensing applications. The zero-cross over input stage provides identical AC and DC performance for both low and high-side sensing applications, thus making OPAx323 the best choice for current sensing in a variety of end equipments such as the solar string inverters, power delivery, grid, and EV infrastructure. Precision transimpedance and voltage gain applications are well served with a low input bias current (0.5 pA typical, 20 pA maximum), a good PSRR (20 µV/V maximum), CMRR (100 dB minimum), and A_{OL} (114 dB minimum). The device has 60° of typical phase margin with no load and drives up to 75 pF with a phase margin of 35°.

OPAx323 has an internal current limit that enables additional robustness when operating with high output current while driving smaller output impedance like 68 Ω, 128 Ω, and 256 Ω loads in audio applications. OPAx323 can swing very close to the rails and has a short circuit current of ±80 mA minimum at 5.5-V power supply. OPAx323S devices provide shutdown functionality for additional power savings and help disable the amplifier when idle. These op amps feature an integrated radio frequency immunity (RFI) and electro-magnetic interference (EMI) rejection filter, unity-gain stability, and no-phase reversal in input overdrive conditions.

7.2 Functional Block Diagram
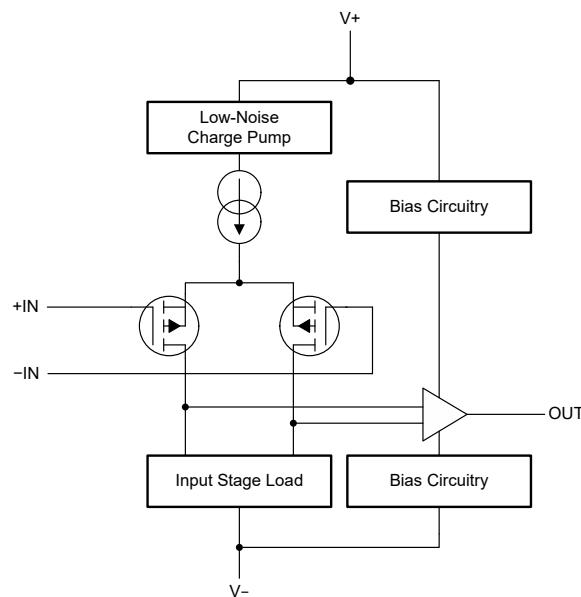
7.3 Feature Description

7.3.1 Operating Voltage

The OPAx323 series of operational amplifiers is fully specified from 1.8 V to 5.5 V and is designed for amplifier operation from 1.7 V to 1.8 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical Characteristics* section. TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Please ensure that C_{BYP} is placed as close to the device as possible and the power supply trace routes through C_{BYP} before reaching the amplifier power supply terminals.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPAx323 series extends beyond the supply rails with a common-mode rejection ratio (CMRR) of 100 dB minimum at 5.5 V as specified in *Electrical Characteristics*. The device is designed to have a good performance of 85 dB minimum CMRR even when operating at an ultra-low supply voltage of 1.8 V. This is made possible by using a zero-cross input stage architecture for the amplifier input pair.

7.3.3 Rail-to-Rail Output

OPAx323 delivers a robust output drive capability. An output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. The device is designed to have a minimum output short circuit current of ±80 mA, making the device an excellent choice for audio driver applications at room temperature and at 5.5 V. For resistive loads up to 2 kΩ and a power supply of 5.5 V, the output swings within a maximum of 55 mV to either supply rail, thereby using almost the entire input range of an ADC in ADC driver applications.

7.3.4 Common-Mode Rejection Ratio (CMRR)

OPAx323 achieves excellent DC and AC CMRR performance. The device is designed to have a DC CMRR performance at two supply voltages (5.5 V and 1.8 V) for the entire operating temperature range (–40°C to 125°C). DC CMRR is specified for common-mode beyond rails over a input voltage range of (V–) – 0.2 V ≤ V_{CM} ≤ (V+) + 0.15 V for 5.5 V operation and (V–) – 0.1 V ≤ V_{CM} ≤ (V+) + 0.05 V for 1.8 V operation. AC CMRR is shown in *Typical Characteristics* and is subject to the routing of input traces on the PCB board. For good performance, maintain a short and symmetrical input trace for the two amplifier input terminals.

7.3.5 Capacitive Load and Stability

OPAx323 is designed for use in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the device can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation.

An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operating at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the OPAx323 has a phase margin of 50° with 30 pF of capacitive load. It remains stable with pure capacitive loads up to approximately 75 pF with acceptable phase margin of 35° and has no sustained oscillations up to 150 pF. The equivalent series resistance (ESR) of some very large capacitors (greater than 1 µF) is sometimes sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10 Ω to 50 Ω) in series with the output, as shown in Figure 7-1. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. This is usually the circuit configuration used in ADC driver application with C_{load} serving as a charge bucket for the ADC sampling capacitor.
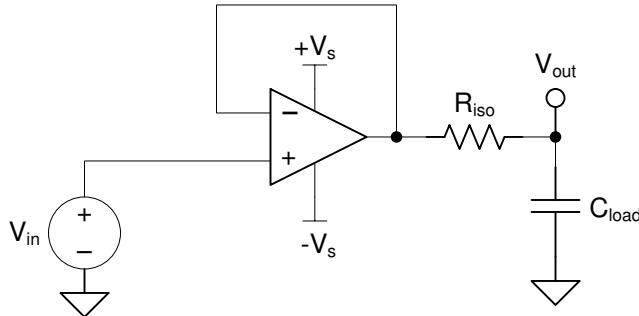
Figure 7-1. Improving Capacitive Load Drive

7.3.6 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output stage of the operational amplifier enters a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After one of the outputs enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time.

The overload recovery time for the OPAx323 family is designed to be approximately 130 ns typical.

7.3.7 ESD and Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and relevance to an electrical overstress event is helpful. Figure 7-2 shows the ESD circuits contained in the OPAx323 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the input and output pins meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Note that the OPAx323 features no current-steering diodes connected between the input and positive power-supply pin.

Product Folder Links: *OPA4323 OPA323 OPA2323*
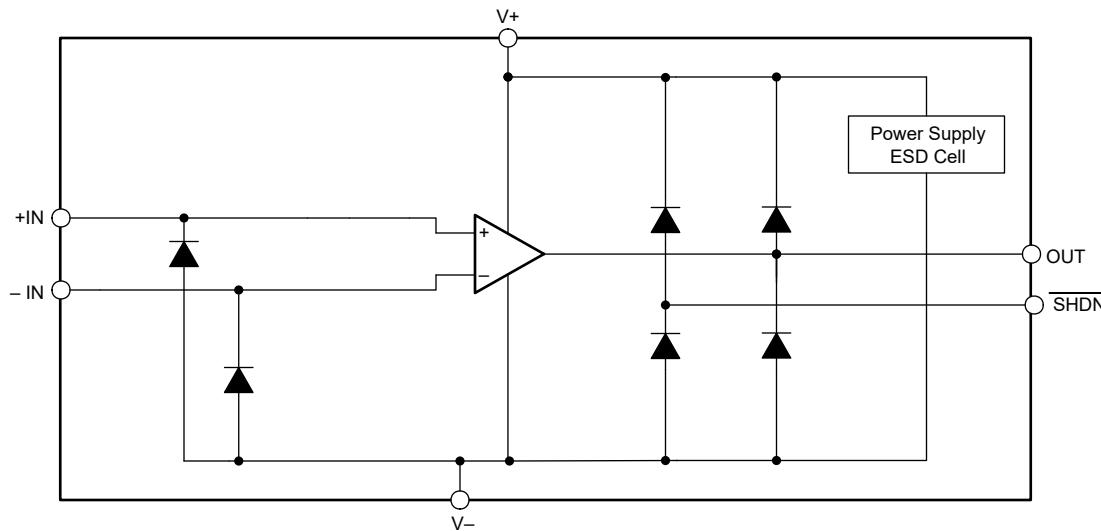
Figure 7-2. Equivalent Internal ESD Circuitry

7.3.8 Input ESD Protection

The OPAx323 family incorporates internal ESD protection circuits on all pins. For inputs, this protection primarily consists of fail safe ESD input structures which feature no current-steering diodes connected between the input and positive power-supply pin as shown in the Figure 7-2. This feature is very useful during power sequencing scenarios where input signal can be present before the positive power supply rail. A fail safe input ESD structure prevents any short between inputs and positive power supply. For further details, refer to *Op Amp ESD Protection Structures* application note.

7.3.9 Shutdown Function

The OPAx323S devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the op amp into a low-power standby mode. In this mode, the op amp typically consumes less than 1000-nA at room temperature. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 500-mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to provide for smooth switching characteristics. For optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins must be driven with valid logic signals. A valid logic low is defined as a voltage between V– and (V–) + 0.2 V. A valid logic high is defined as a voltage between (V–) + 1 V and V+. To enable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. TI highly recommends to not leave the shutdown pin floating, but to connect the shutdown pin to a valid high or low voltage. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5 V. Exceeding this voltage level damages the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life. The enable and disable time is targeted to be under 1-µs for full shutdown of all channels. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx323S to operate as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions as any charge on the output capacitor needs to be discharged by any external resistive load or the op-amp. To achieve the 1-µs shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required with no capacitive load.

Product Folder Links: *OPA4323 OPA323 OPA2323*

7.3.10 Packages with an Exposed Thermal Pad

The OPAx323 family is available in packages such as the WQFN-16 (RTE) and WSON-8 (DSG), which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must be connected to V–. Attaching the thermal pad to a potential other then V– is not allowed, and the performance of the device may not be consistent with the *Electrical Characteristics* table when doing so.

7.4 Device Functional Modes

The OPAx323 devices have one functional mode. These devices are powered on as long as the power-supply voltage is between 1.7 V (±0.85 V) and 5.5 V (±2.75 V).

The OPAx323S devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. For more information, see the *Shutdown Function* section.

Product Folder Links: *OPA4323 OPA323 OPA2323*

8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx323 family of rail-to-rail input and output operational amplifiers is specifically designed for variety of high gain and high speed applications. These devices operate from 1.7 V to 5.5 V, are unity-gain stable, and are also an excellent choice for a wide range of general-purpose applications. The output stage is capable of driving small resistive loads connected to any point between V+ and V– as long as the device is not forced into short circuit mode. The input common-mode voltage range includes beyond the rail signal swing and allows the OPAx323 series to be used in many single-supply or dual supply configurations.

8.2 Typical Application

8.2.1 OPAx323 in Low-Side, Current Sensing Application

Figure 8-1 shows the OPA323 configured in a low-side current sensing application.
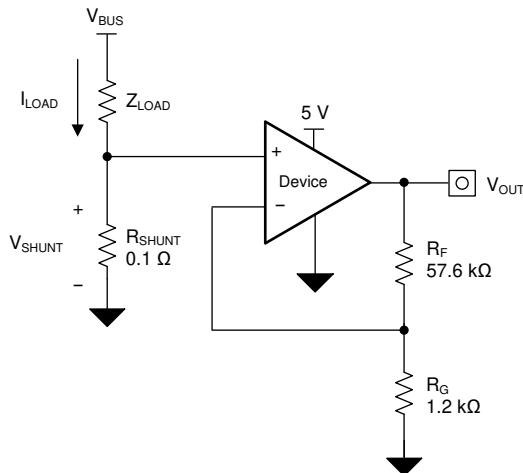
Figure 8-1. OPA323 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Maximum output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 8-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\,mV}{1\,A} = 100\,m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA323 to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the OPA323 to produce the necessary output voltage is calculated using Equation 3.

$$Gain = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{IN\_MAX} - V_{IN\_MIN}} \tag{3}$$

Using Equation 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the OPA323 to 49 V/V.

$$Gain = 1 + \frac{R_F}{R_G} \tag{4}$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. Figure 8-2 shows the measured transfer function of the circuit shown in Figure 8-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; choose an impedance that is best for the system parameters.

8.2.1.3 Application Curve
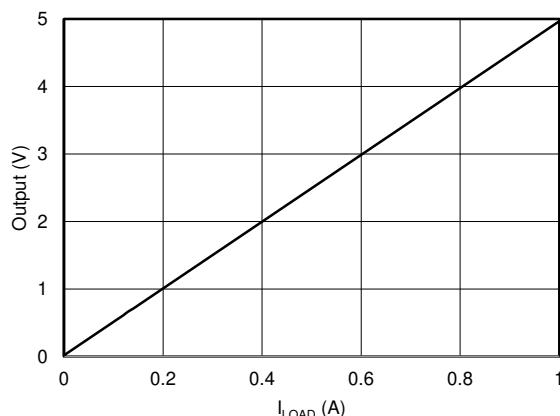
Figure 8-2. Low-Side, Current-Sense Transfer Function

8.3 Power Supply Recommendations

The OPAx323 family is tested for amplifier operation at 1.7 V and it is fully specified from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. *Electrical Characteristics* presents parameters that can exhibit significant variance regarding operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device; for more information, see the *Absolute Maximum Ratings* table.

TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Place the C_{BYP} as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Please ensure the power supply trace routes through C_{BYP} before reaching the amplifier power supply terminals. For more information, see *Layout Guidelines*.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
    - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. One bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, then cross the sensitive trace at a 90 degree angle, which is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in *Layout Example*. Keeping R_1 and R_2 close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example
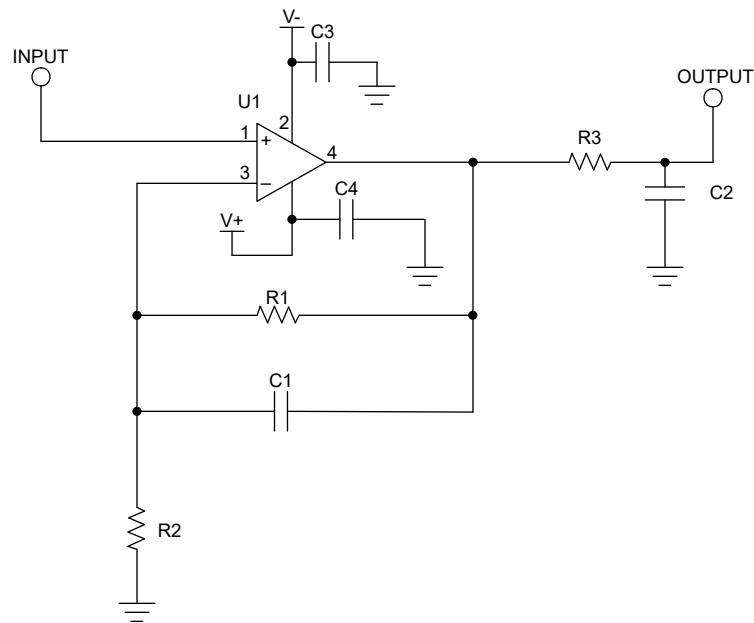
Note: C3 and C4 are C_{BYP} capacitors

**Figure 8-3. Schematic for Noninverting Configuration Layout Example**
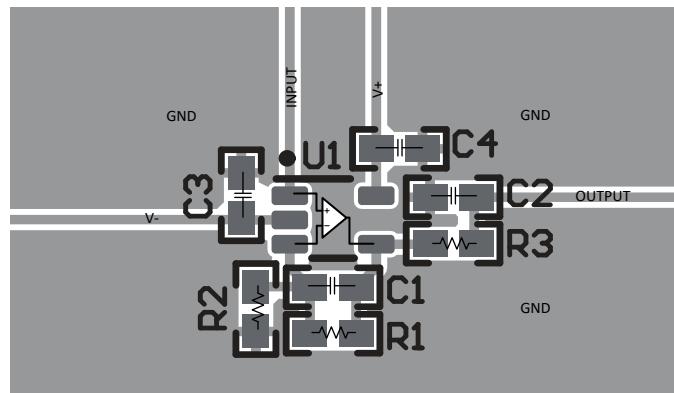
Figure 8-4. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (November 2023)	Page
• Changed the status of the DCK (SC70, 5) OPA323 from: *preview* to: *active* 1	
• Changed the status of the D (SOIC, 8) OPA2323 from: *preview* to: *active* 1	

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2323IDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2323ID	Samples
OPA323IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1RG	Samples
OPA4323IPWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4323PW	Samples
POPA2323IDGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS
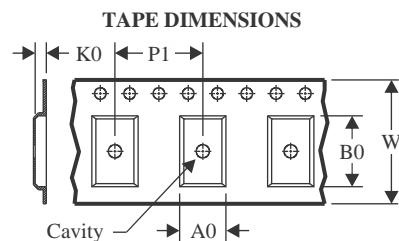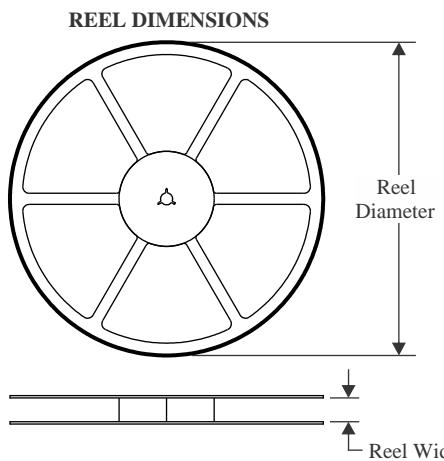
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
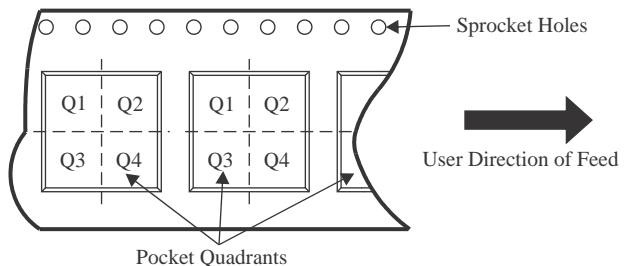
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2323IDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA323IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4323IPWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2323IDR	SOIC	D	8	3000	356.0	356.0	35.0
OPA323IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA4323IPWR	TSSOP	PW	14	3000	356.0	356.0	35.0
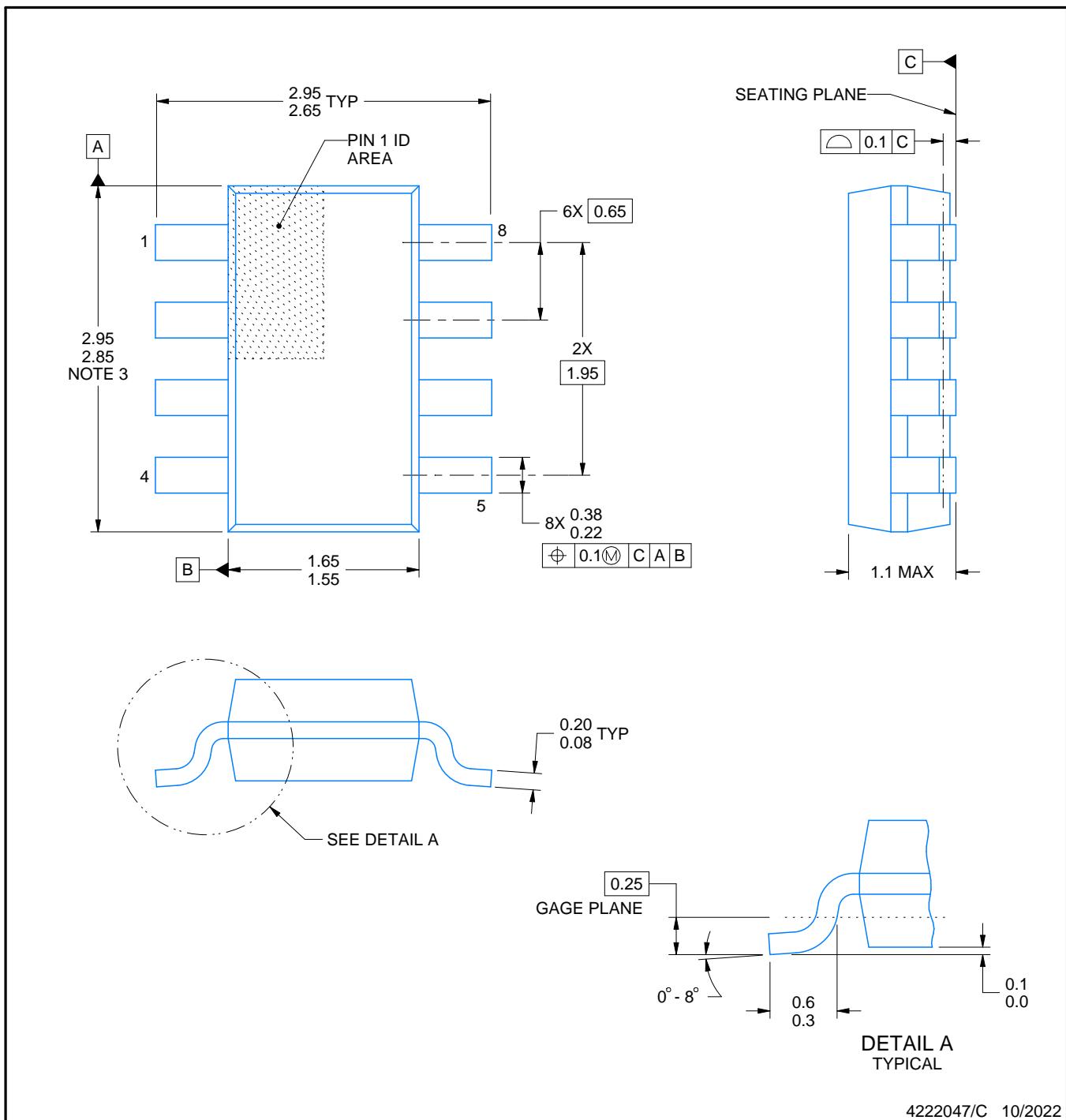
2.95
2.65 TYP

A

PIN 1 ID
AREA

2.95
2.85
NOTE 3

1

4

B

1.65
1.55

6X 0.65

8

2X
1.95

5

8X 0.38
0.22

⊕ 0.1 Ⓜ C A B

C

SEATING PLANE

⌓ 0.1 C

1.1 MAX

0.20
0.08 TYP

SEE DETAIL A

0.25

GAGE PLANE

0°- 8°

0.6
0.3

0.1
0.0

DETAIL A
TYPICAL

4222047/C   10/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

8X (1.05)

SYMM
℄

1

8X (0.45)

8

SYMM
℄

6X (0.65)

4

5

(R0.05)
TYP

(2.6)
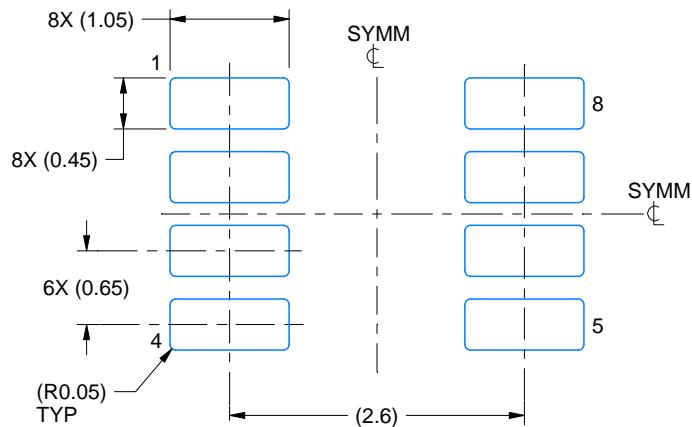
LAND PATTERN EXAMPLE
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING
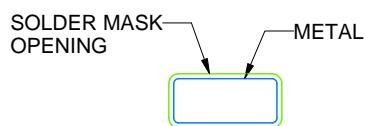
NON SOLDER MASK
DEFINED
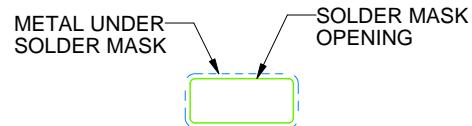
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C   10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.05)

SYMM

(R0.05) TYP

1

8X (0.45)

SYMM

6X (0.65)

4

5

8

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X
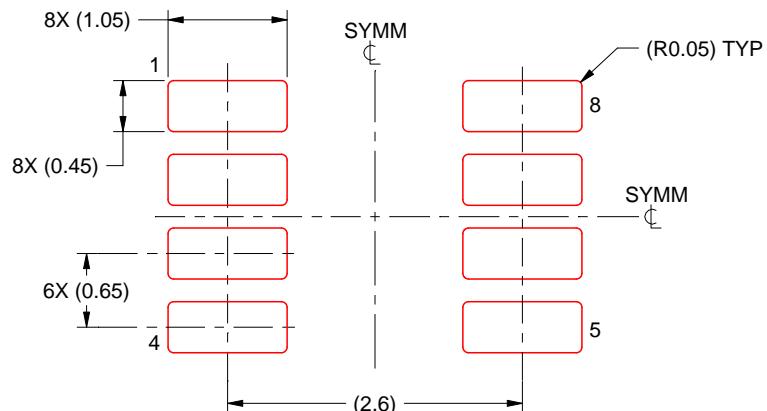
4222047/C   10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

RTE 16

3 x 3, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
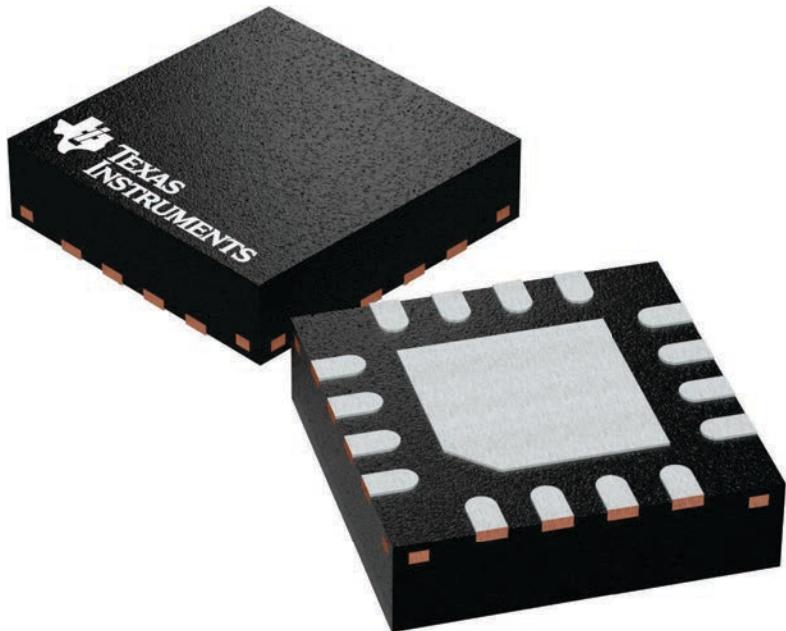
4225944/A
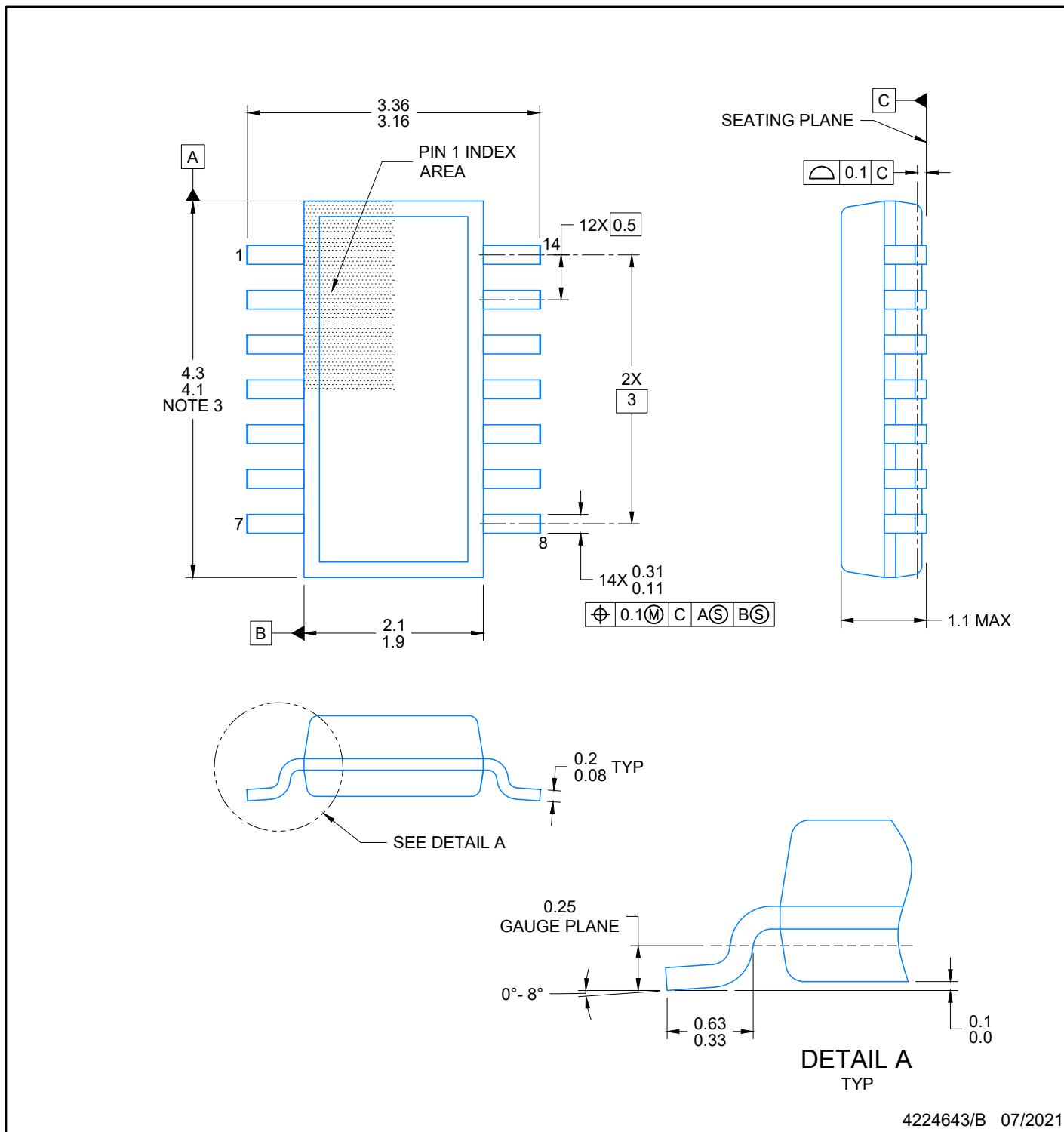
3.36
3.16

A

PIN 1 INDEX
AREA

SEATING PLANE

C

0.1 C

1

12X 0.5

14

4.3
4.1
NOTE 3

2X
3

7

8

14X 0.31
0.11

B

2.1
1.9

⌖ 0.1 Ⓜ C AⓈ BⓈ

1.1 MAX

0.2
0.08 TYP

SEE DETAIL A

0.25
GAUGE PLANE

0°- 8°

0.63
0.33

0.1
0.0

DETAIL A
TYP

4224643/B   07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

SYMM

14X (1.05)

1

14

14X (0.3)

SYMM

12X (0.5)

7

8

(R0.05) TYP

(3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224643/B   07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SYMM

14X (1.05)

1

14

14X (0.3)

SYMM

12X (0.5)

7

8

(R0.05) TYP

(3)
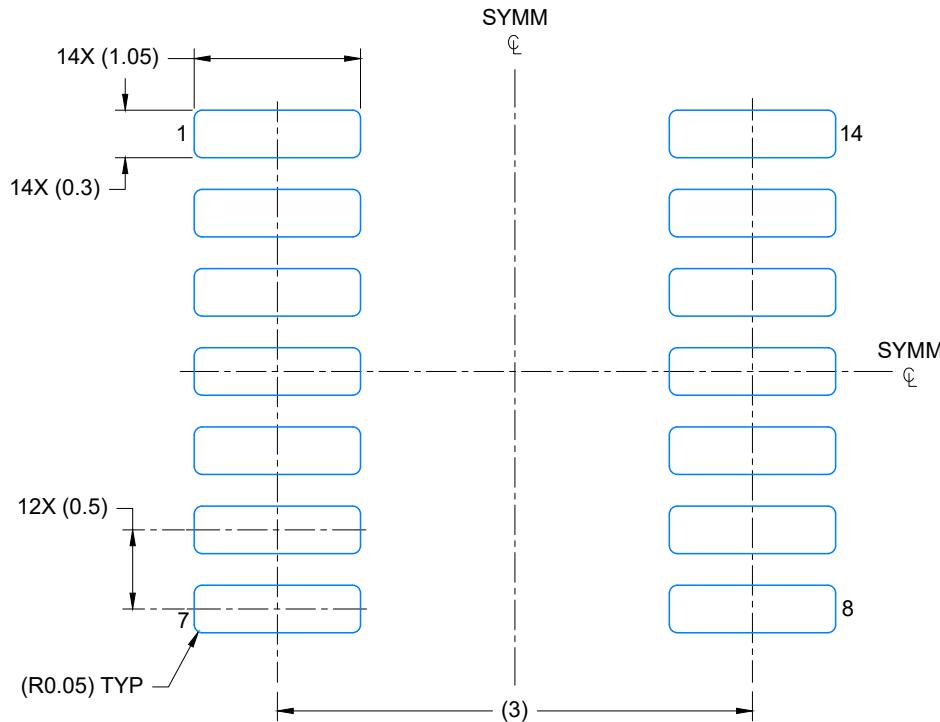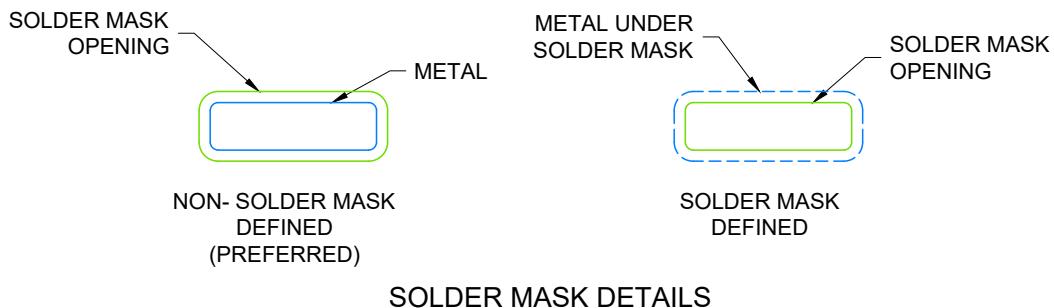
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B   07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
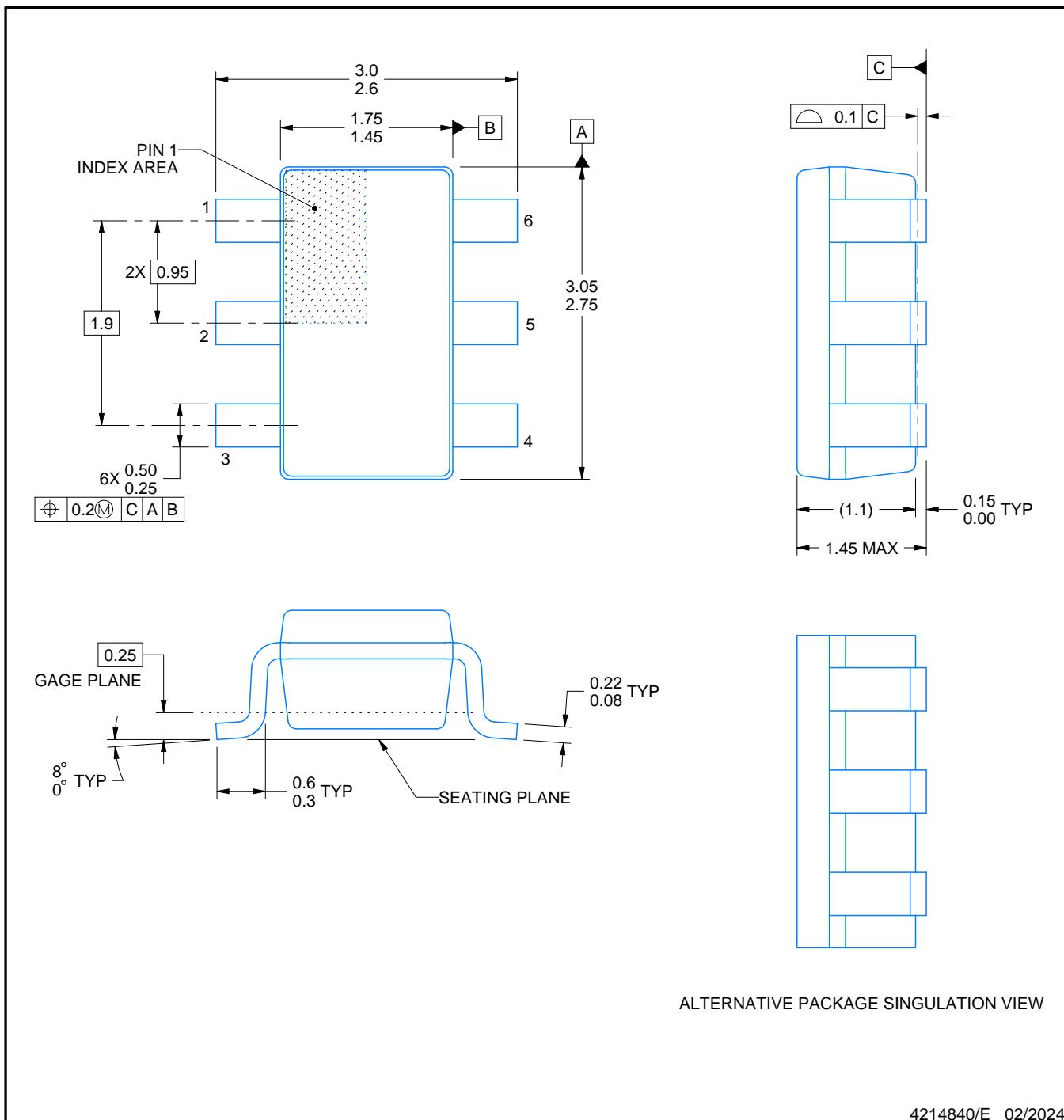
4214840/E   02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

PKG ℄

6X (1.1)

1

6X (0.6)

2

SYMM ℄

2X (0.95)

3

(R0.05) TYP

6

5

4

(2.6)
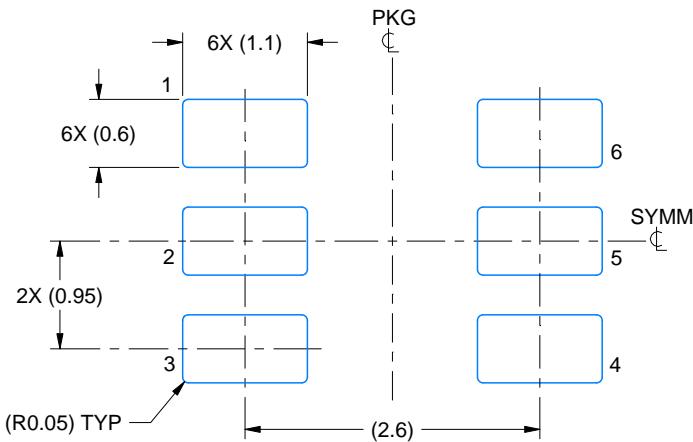
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED
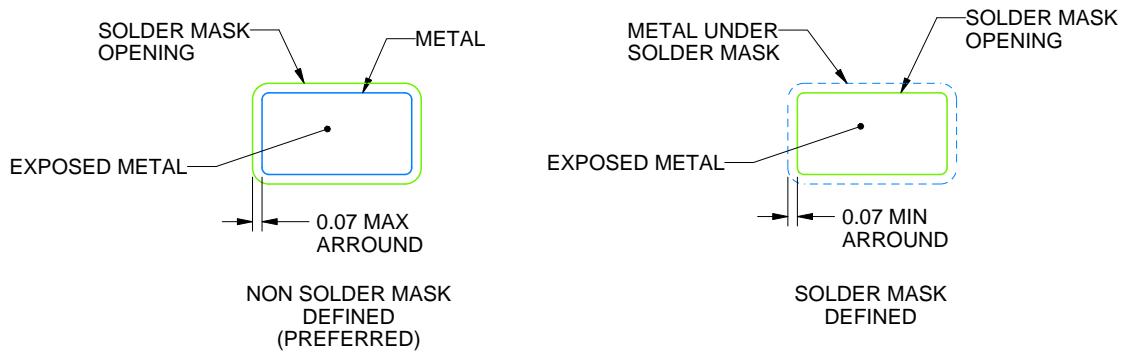
SOLDER MASK DETAILS

4214840/E   02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

6X (1.1)

1

6X (0.6)

2

SYMM

6

5

2X(0.95)

3

4

(R0.05) TYP

(2.6)
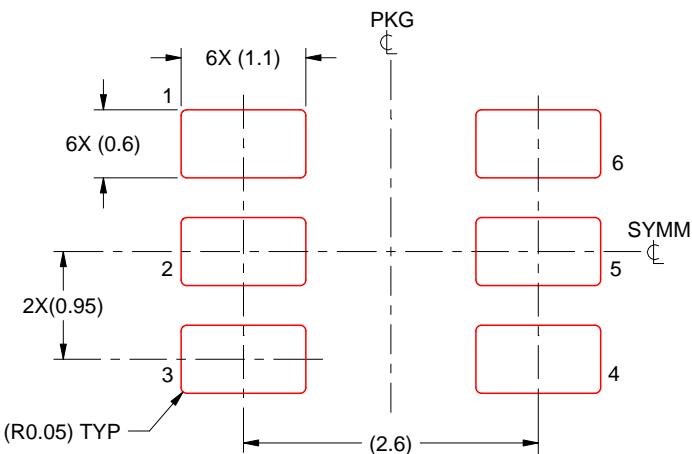
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PIN 1
INDEX AREA

2.4
1.8

1.4
1.1

B

A

1

5

2X 0.65

1.3

2

NOTE 4

(0.15)

(0.1)

1.3

2.15
1.85

3

4

5X 0.33
0.15

⊕ | 0.1 Ⓜ | C | A | B
NOTE 5

C

△ | 0.1 | C

1.1 MAX

(0.9)

0.1
0.0 TYP

0.15

GAGE PLANE

0.22
0.08 TYP

8°
0° TYP

0.46
0.26 TYP

SEATING PLANE

4214834/D 07/2023
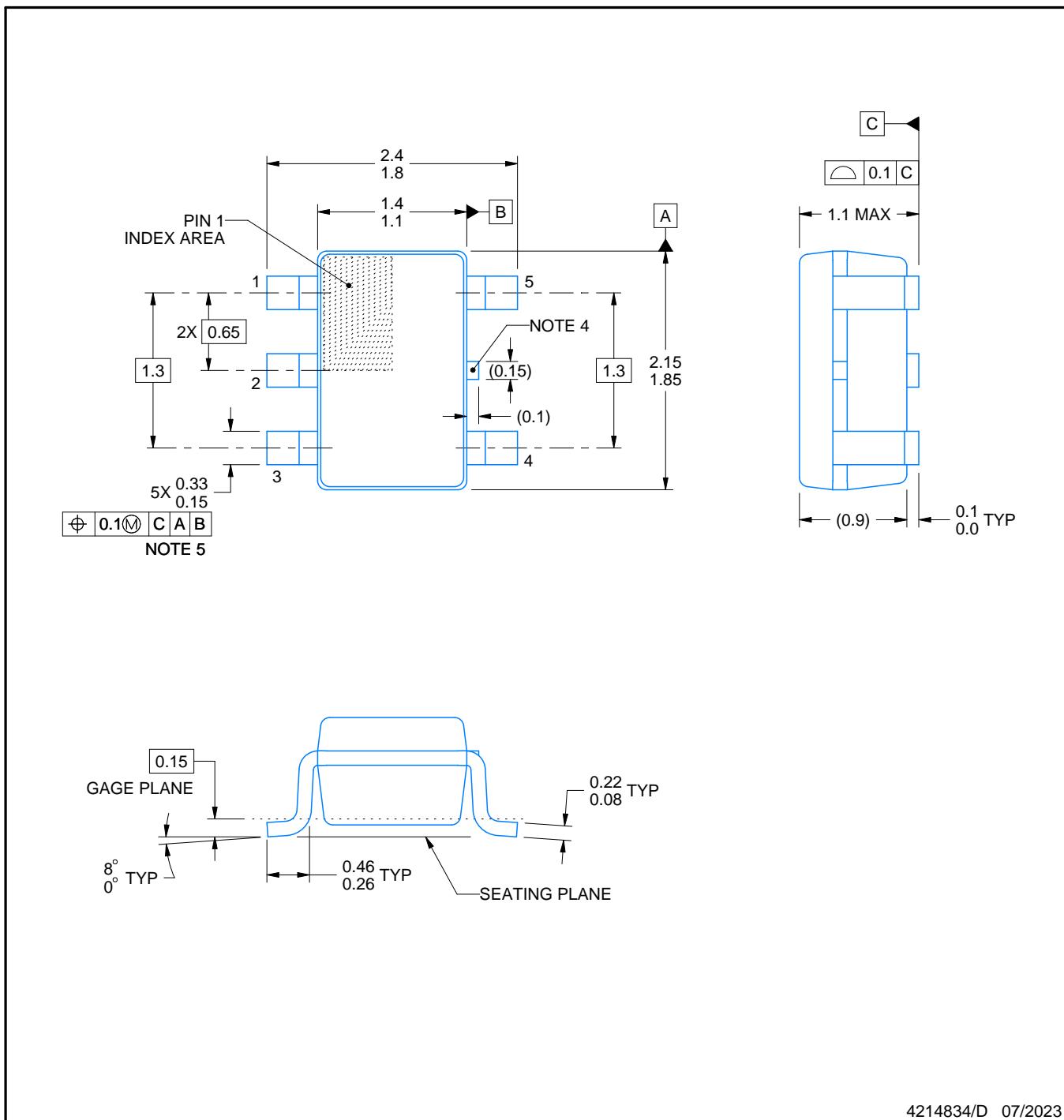
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.

5X (0.95)

PKG ₵

1

5X (0.4)

5

SYMM ₵

2

(1.3)

2X (0.65)

3

4

(R0.05) TYP

(2.2)
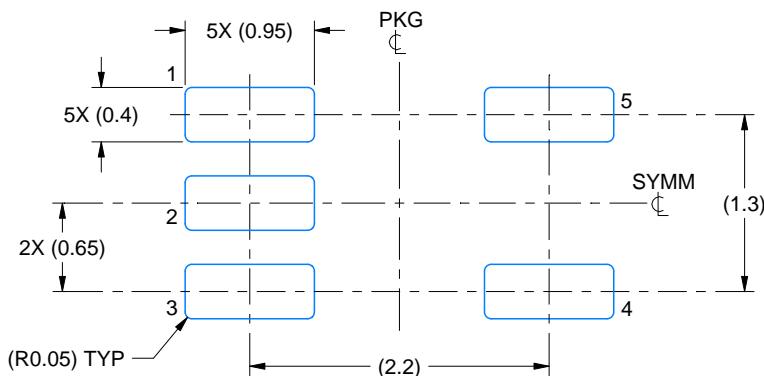
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED
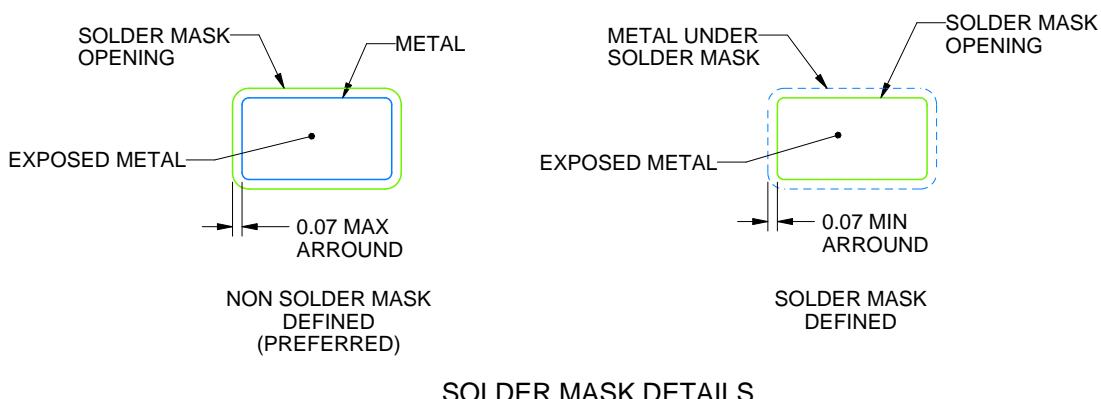
SOLDER MASK DETAILS

4214834/D   07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
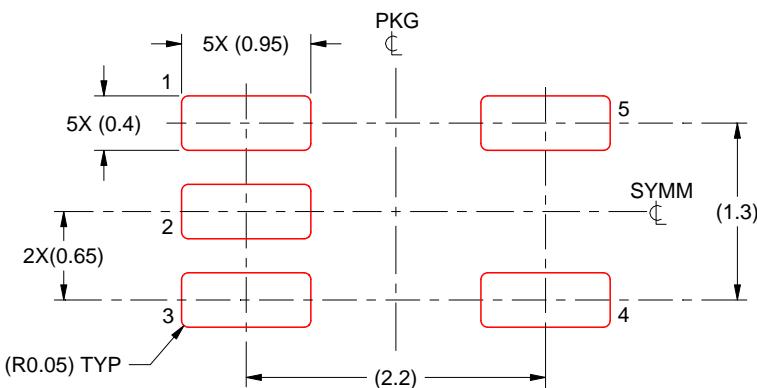
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D   07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE
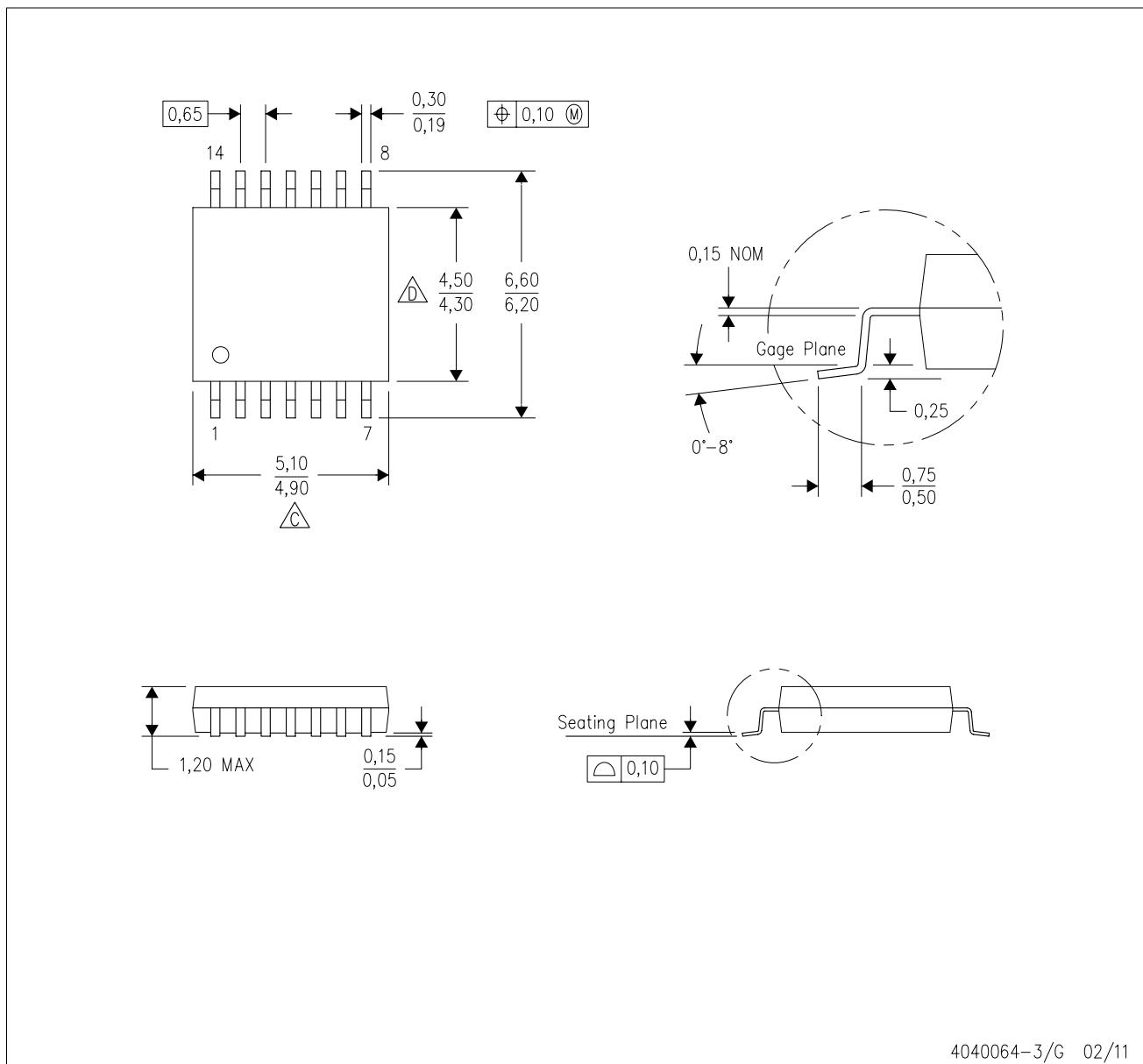
0,65

0,30 / 0,19

⊕ 0,10 Ⓜ

14   8

4,50 / 4,30 (D)

6,60 / 6,20

1   7

5,10 / 4,90 (C)

0,15 NOM

Gage Plane

0,25

0°–8°

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane

⌓ 0,10

4040064–3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
        B. This drawing is subject to change without notice.
        (C) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        (D) Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO–153

RUG (R−PQFP−N10)   PLASTIC QUAD FLATPACK

Pin 1 Index Area

2,05 / 1,95   A

B

1,55 / 1,45

9 8 7 6

10   5

1 2 3 4

0,40 / 0,34

0,05 C

Seating Plane

0,05 / 0,00

C

Seating Height

1,50

0,50

8X 0,40 / 0,30

Pin 1 Identifier
0,10 X 45°

1 2 3 4

10   5

2X 0,35 / 0,25

9 8 7 6

2X 0,45 / 0,35

4X 0,30 / 0,20

4X 0,25 / 0,15

10X

⊕ | 0,10 Ⓜ | C | A | B
  | 0,05 Ⓜ | C
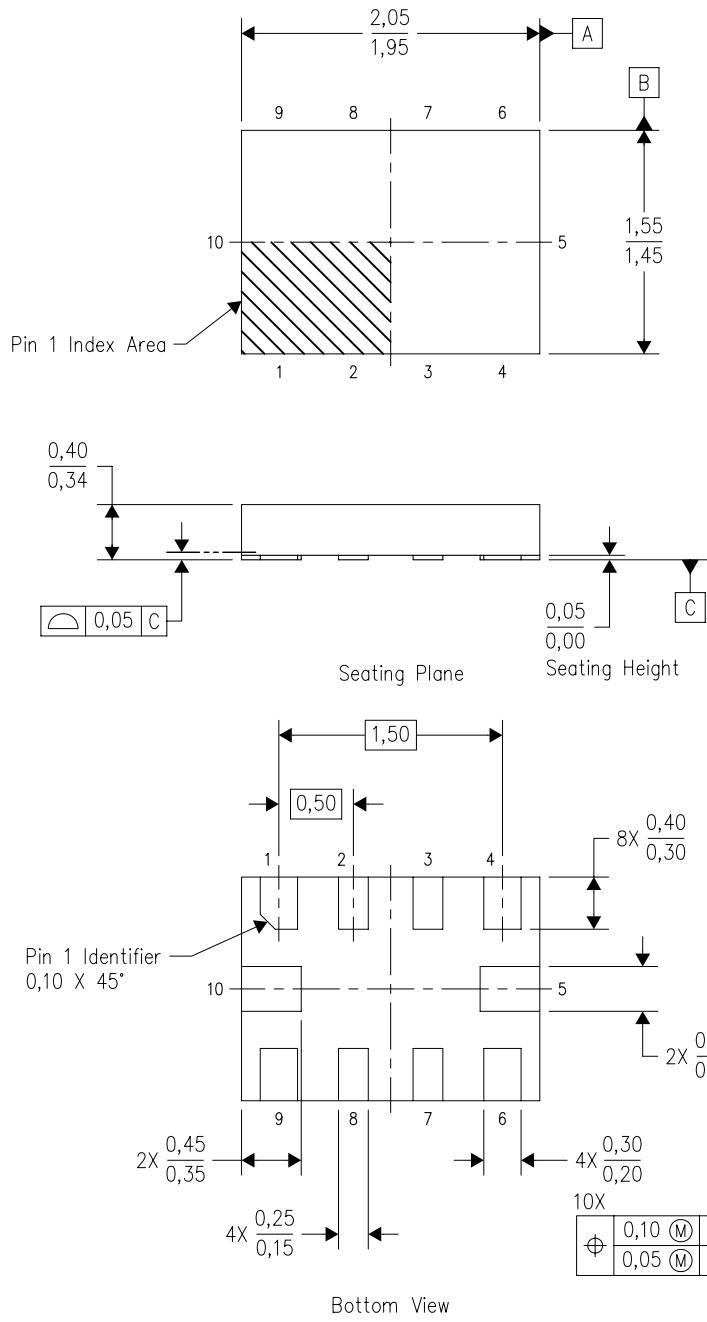
Bottom View

4208528−3/B 04/2008

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No−Lead) package configuration.
   D. This package complies to JEDEC MO−288 variation X2EFD.

4214825/C   02/2019
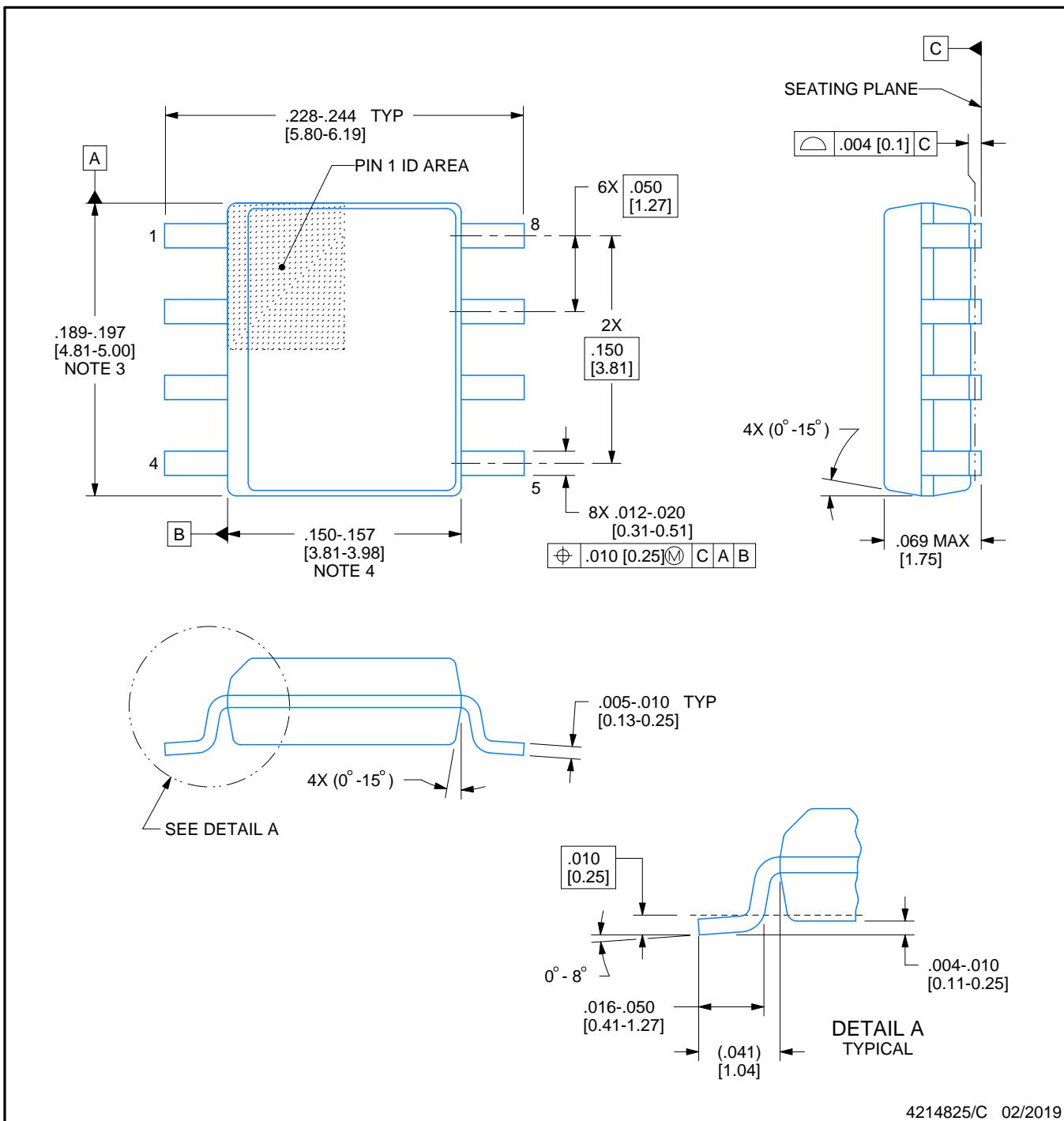
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
₵

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
₵

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL ─

SOLDER MASK
OPENING

SOLDER MASK ─
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND
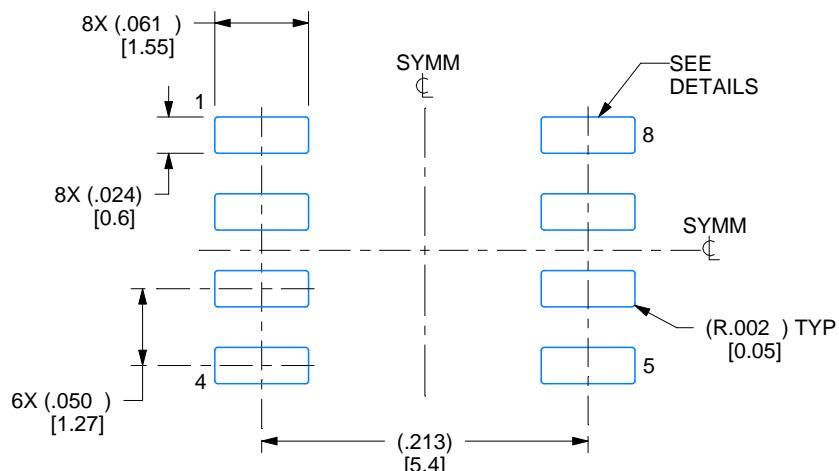
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
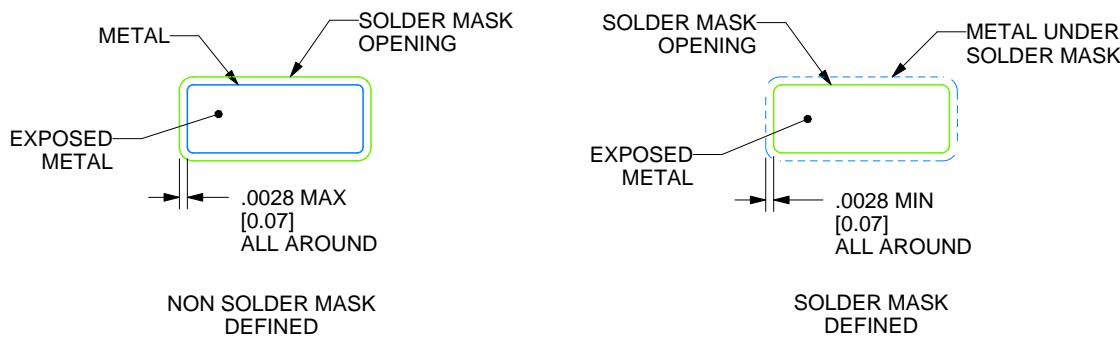
SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

SYMM
℄

8

SYMM
℄

(R.002) TYP
[0.05]

5

6X (.050)
[1.27]

4

(.213)
[5.4]
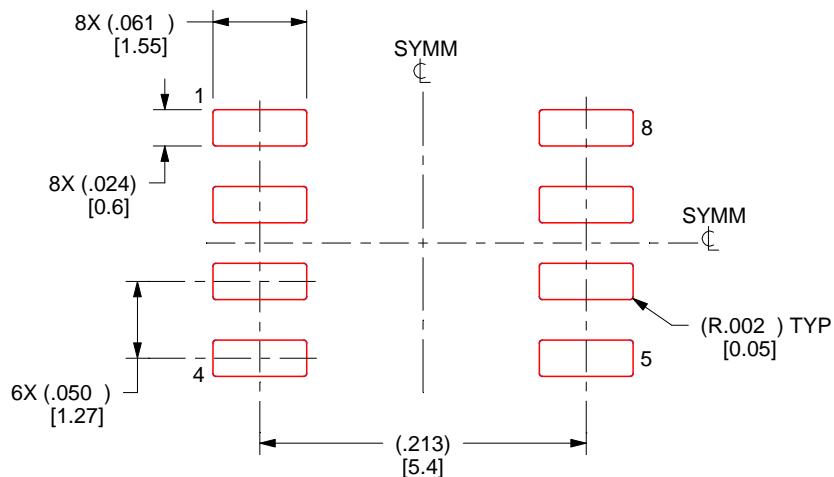
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0,65

8   5

0,38
0,25   ⊕ 0,13 Ⓜ

D▷ 3,10
2,90   5,05
4,75

1   4
C▷
3,10
2,90

0,23
0,13

Gauge Plane

0°−8°   0,25

0,70
0,40

1,10 MAX   0,15
0,05

Seating Plane

△ 0,10

4073329/E 05/06
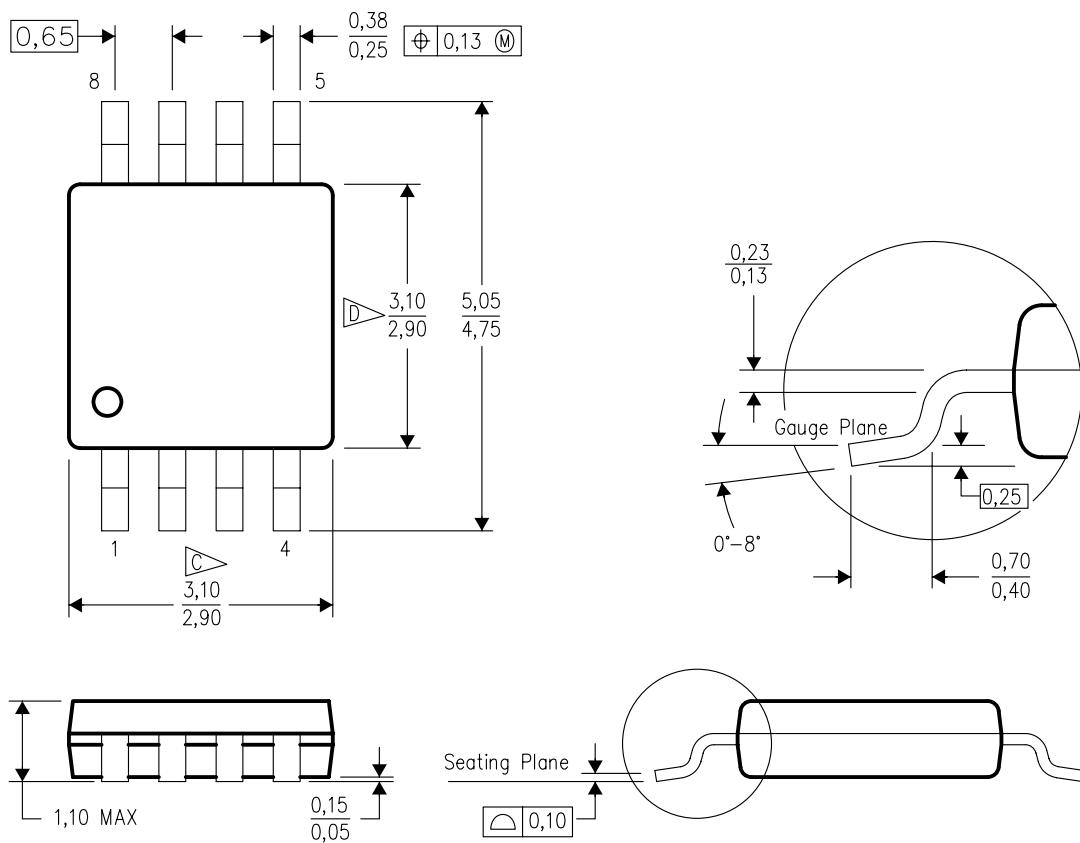
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
     C▷ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0.15 per end.
     D▷ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
        E. Falls within JEDEC MO−187 variation AA, except interlead flash.

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