Qualcomm

Qualcomm® QCC740

Tri-Radio SoC

Fully integrated, high-performance 1x1 Wi-Fi 6, Bluetooth® 5.3 qualified, and IEEE 802.15.4 SoC with stacked memory options for IoT applications.

The QCC740 is a tri-radio chipset integrating 1x1 Wi-Fi 6, Bluetooth 5.3 qualifications, and IEEE 802.15.4 (Thread and Zigbee-ready) powered by a 32-bit RISC-V MCU up to 325 MHz and stacked memory (pSRAM and NOR flash).

Unlike other Wi-Fi/Bluetooth 5.3 qualified/15.4 combination chipsets on the market, QCC740 is integrated with a wide array of on-chip features, including a powerful 32-bit RISC-V processor with an FPU and DSP running up to 325 MHz, 484 KB SRAM, 48 KB cache, and 128 KB ROM, as well as an optional 4/8/16 MB pSRAM and 8 MB NOR flash System-in-Package (SiP). It also includes multimedia features such as audio and video codec and interfaces, and 35x multiplexed GPIO-rich peripherals. Its all-in-one design and capabilities contribute to reduced costs and enhanced performance, making it an attractive choice for IoT edge devices requiring a single-chip solution.

QCC740 operates in hostless mode, capable of running both the protocol stack all the way to the application level as well as IoT applications without requiring an external MCU. Built on FreeRTOS, its software SDK will be open-sourced on CodeLinaro coupled with the Microsoft Visual Studio Code (VS Code) IDE market extension to facilitate rapid IoT application development. It can also be used as an IoT connectivity transceiver in hosted mode (both RCP and NCP) with an external host.

Highlights

Full radio integration

QCC740 integrates all of the following radios required for IoT connectivity: 1x1 Wi-Fi 6, Bluetooth 5.3 qualified dual mode (BR/EDR and LE with coded PHY), and IEEE 802.15.4 (Thread and Zigbee-ready). It will support Matter over Wi-Fi, Thread, as well as Ethernet with BLE commissioning capability.

High computing power

In addition to radio integration, QCC740 also has a powerful 32-bit RISC-V microcontroller up to 325 MHz with a DSP and FPU at its core. It also has the option to add stacked memory like pSRAM and NOR flash to boost computing capability.

High security

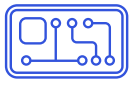
QCC740 has a built-in security acceleration engine, supporting both symmetric and asymmetric algorithms. It provides security services like Secure Boot and Secure Debug, and can support public key accelerators, TRNG, and QSPI (XiP) on-the-fly AES decryption. It is qualified for PSA Certified Level One.

Rich peripherals and multimedia support

QCC740 has 35x on-chip GPIO pins that can be multiplexed to support rich peripheral interfaces like QSPI, SDIO, SD card, SPI, UART, I2C, I2S, PWM, 12-bit ADC, 12-bit DAC, IR remote, RMII (10/100 Ethernet), CAN (ISO11898), DVP camera, and DBI display. It has built-in motion JPEG to support 720p video codec as well as MIC input with 8/12/16/22.05/24/32/44.1/48 KHz audio sampling and speaker output.

User-friendly development environment and tools

QCC740 will be provided with an open-source software SDK available on CodeLinaro, the VS Code-based IDE supported by size- and cost-optimized modules as well as associated development kits.



87-75957-1 Rev. D

Target Applications

- Smart Appliances
- Medical Devices
- Industrial IoT
- Smart Home Devices
- IoT Hubs/Gateways

Features

- Full radio integration to address all IoT connectivity needs
- High-performance 32-bit RISC-V MCU with large memory resource and a stacked memory SiP option
- Advanced hardware-based security featuring public key accelerator, TRNG, and QSPI (XiP) on-the-fly AES decryption
- Secure Boot and Secure Debug
- Rich peripheral interfaces including Ethernet, CAN, etc.
- Direct camera interface (DVP) and display control (DBI)
- Multimedia features like motion JPEG (720p) and MIC and speaker support
- Support hostless and hosted (RCP and NCP) operation modes
- Open-source support with SDK on CodeLinaro, VS Code IDE market extension, as well as modules and associated development kits

Ordering Information

Product	Part Numbers
QCC740	QCC-743-1-MQFN40-MT-00-0 (bulk) QCC-743-1-MQFN40-TR-00-0 (tape and reel) QCC-744-2-MQFN56-MT-00-0 (bulk) QCC-744-2-MQFN56-TR-00-0 (tape and reel)

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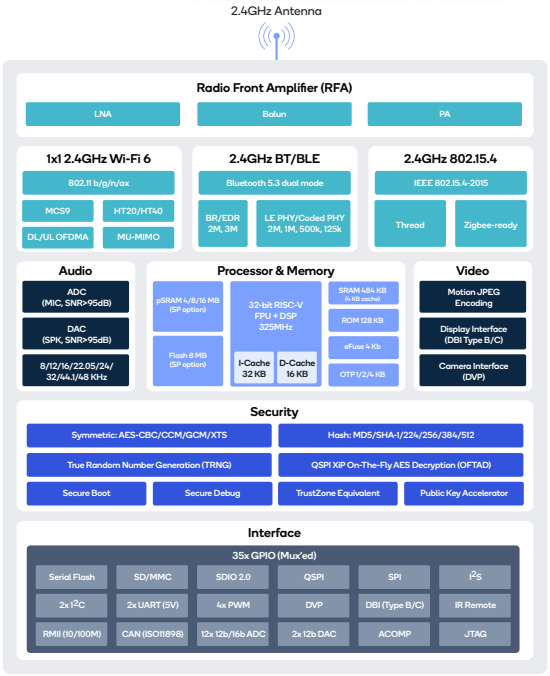
Block Diagram



Specifications

CPU	32-bit RISC-V @ 325 MHz with DSP and FPU 128 KB ROM, 4 Kb eFuse, and 1/2/4 KB OTP 484 KB on-chip SRAM (32 KB I-Cache and 16 KB D-Cache) 4/8/16 MB pSRAM SiP (optional) 8 MB NOR flash SiP (optional)
Bluetooth	Bluetooth 5.3 qualified dual mode (BR/EDR and LE with coded PHY)
Wi-Fi	1x1, 2.4GHz, 802.11b/g/n/ax
Security Support	Cryptographic Accelerator, Secure Boot, Qualcomm® Trusted Execution Environment (TEE), Secure Debug, PSA Certified Level One
Interfaces & Peripherals	Up to 35x GPIO (mux'ed) SD/MCC/SF, SDIO, QSPI, SPI, I2C, I2S, UART, PWM, ADC/DAC, CAN, RMII
Package Type	QFN-40, 5.0 x 5.0 x 0.85 mm, 0.4 mm pitch QFN-56, 7.0 x 7.0 x 0.85 mm, 0.4 mm pitch
Temperature	-40~+105° C
Voltage	Input Voltage: 2.97~3.63V I/O Voltage: 1.8V/3.3V