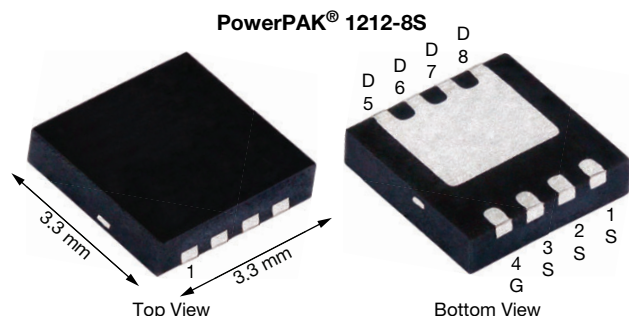


N-Channel 150 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	150
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.042
Q_g typ. (nC)	8.5
I_D (A)	25.5 ^a
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS72DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	150	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	25.5	A
	$T_C = 70^\circ\text{C}$		20.4	
	$T_A = 25^\circ\text{C}$		7 ^{b, c}	
	$T_A = 70^\circ\text{C}$		5.6 ^{b, c}	
Pulsed drain current ($t = 100 \mu\text{s}$)		I_{DM}	50	A
Continuous source-drain diode current	$T_C = 25^\circ\text{C}$	I_S	54.8	
	$T_A = 25^\circ\text{C}$		4.2 ^{b, c}	
Single pulse avalanche current	$L = 0.1 \text{ mH}$	I_{AS}	20	mJ
Single pulse avalanche energy		E_{AS}	20	
Maximum power dissipation	$T_C = 25^\circ\text{C}$	P_D	65.8	W
	$T_C = 70^\circ\text{C}$		42.1	
	$T_A = 25^\circ\text{C}$		5.1 ^{b, c}	
	$T_A = 70^\circ\text{C}$		3.2 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^c			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM
Maximum junction-to-ambient ^b	$t \leq 10 \text{ s}$	R_{thJA}	20	25
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.5	1.9

Notes

- $T_C = 25^\circ\text{C}$
- Surface mounted on 1" x 1" FR4 board
- $t = 10 \text{ s}$
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 65°C/W

FEATURES

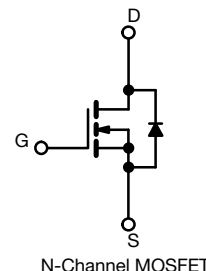
- TrenchFET® with ThunderFET technology optimizes balance of $R_{DS(on)}$, Q_g , Q_{sw} , and Q_{oss}
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Primary side switching
- Synchronous rectification
- DC/DC converter
- Motor drive control
- Load switch



N-Channel MOSFET



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	150	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 mA	-	92	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-7.1	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 150 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 150 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	V _{DS} ≤ 10 V, V _{GS} = 10 V	20	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 7 A	-	0.035	0.042	Ω
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7 A	-	16	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz	-	550	-	pF
Output capacitance	C _{oss}		-	120	-	
Reverse transfer capacitance	C _{rss}		-	6	-	
Total gate charge	Q _g	V _{DS} = 75 V, V _{GS} = 10 V, I _D = 7 A	-	10.85	22	nC
		V _{DS} = 75 V, V _{GS} = 7.5 V, I _D = 7 A	-	8.5	13	
Q _{gs}	-		3	-		
Q _{gd}	-		3	-		
Output charge	Q _{oss}	V _{DS} = 75 V, V _{GS} = 0 V	-	27.7	42	
Gate resistance	R _g	f = 1 MHz	0.24	1.2	2.4	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 75 V, R _L = 13.4 Ω, I _D ≅ 5.6 A, V _{GEN} = 10 V, R _g = 1 Ω	-	18	36	ns
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	9	18	
Turn-on delay time	t _{d(on)}	V _{DD} = 75 V, R _L = 13.4 Ω, I _D ≅ 5.6 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	20	40	
Rise time	t _r		-	8	16	
Turn-off delay time	t _{d(off)}		-	25	50	
Fall time	t _f		-	11	22	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	54.8	A
Pulse diode forward current	I _{SM}		-	-	50	
Body diode voltage	V _{SD}	I _S = 5.6 A, V _{GS} = 0 V	-	0.8	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 5.6 A, di/dt = 100 A/μs, T _J = 25 °C	-	60	120	ns
Body diode reverse recovery charge	Q _{rr}		-	133	266	nC
Reverse recovery fall time	t _a		-	50	-	ns
Reverse recovery rise time	t _b		-	10	-	

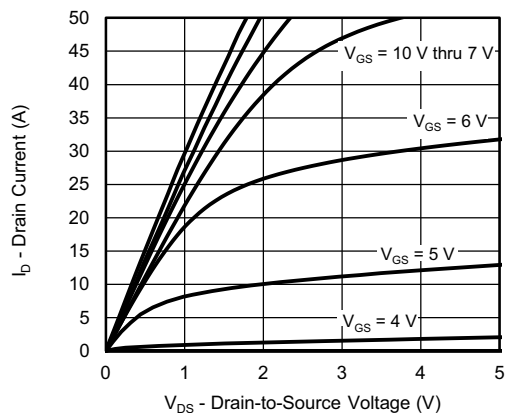
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

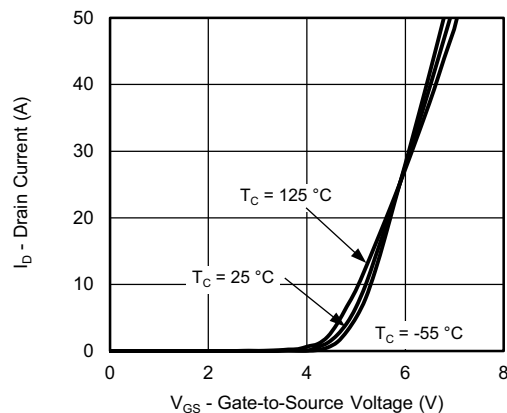
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



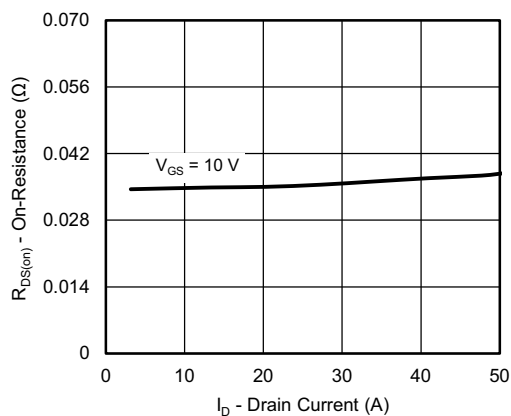
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



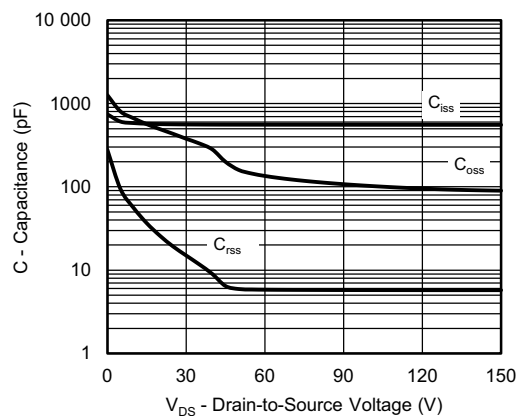
Output Characteristics



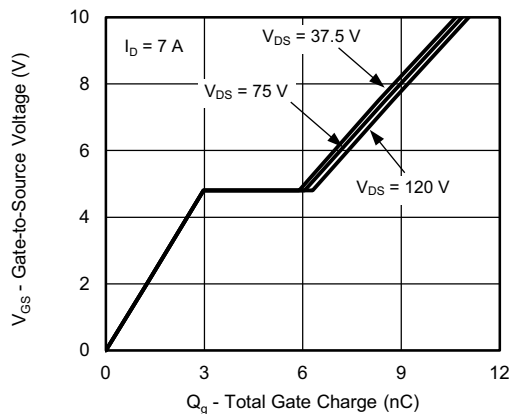
Transfer Characteristics



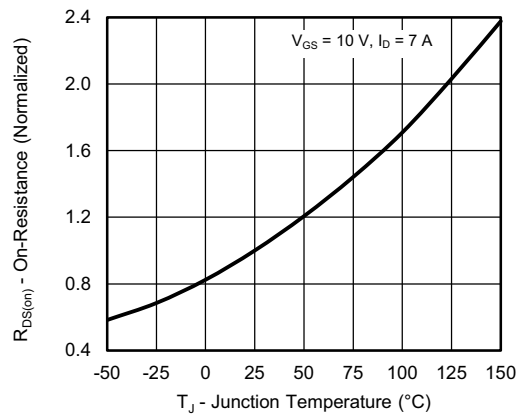
On-Resistance vs. Drain Current and Gate Voltage



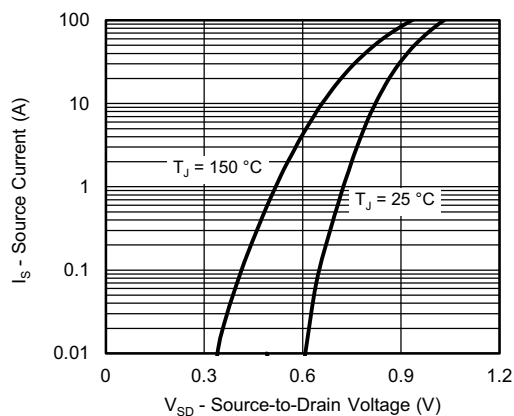
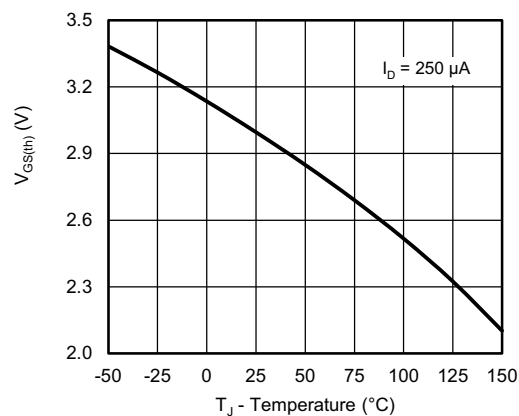
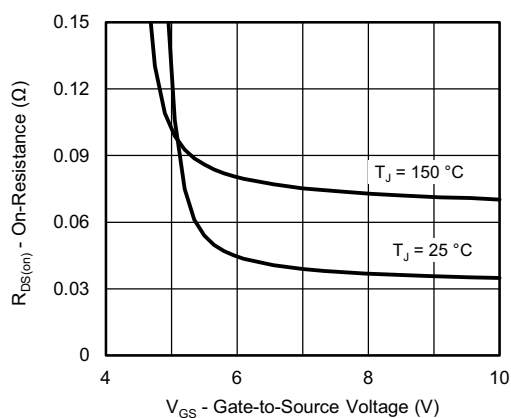
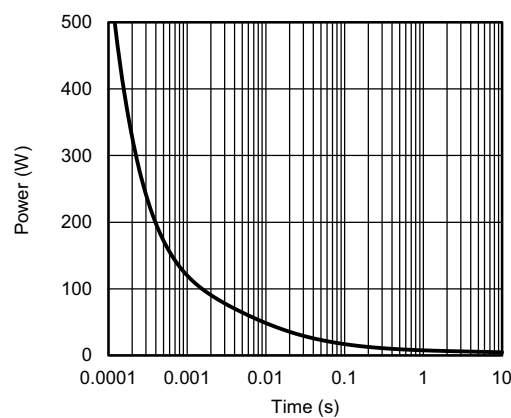
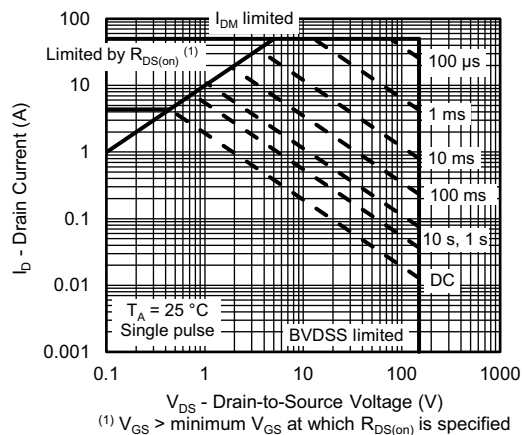
Capacitance

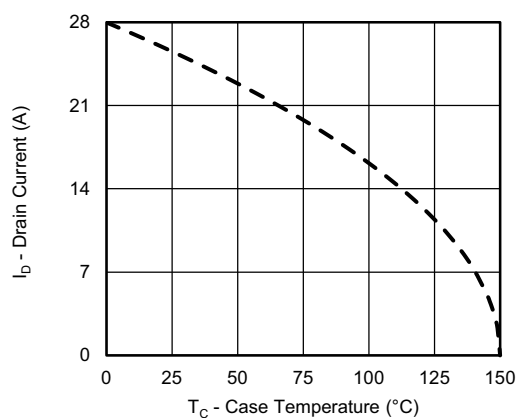
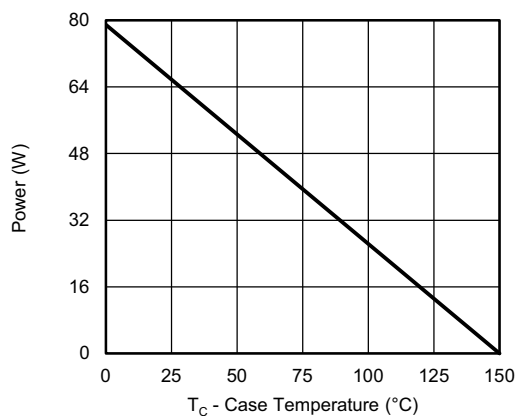
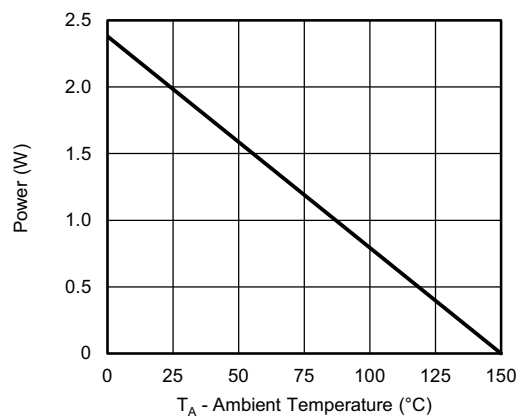


Gate Charge

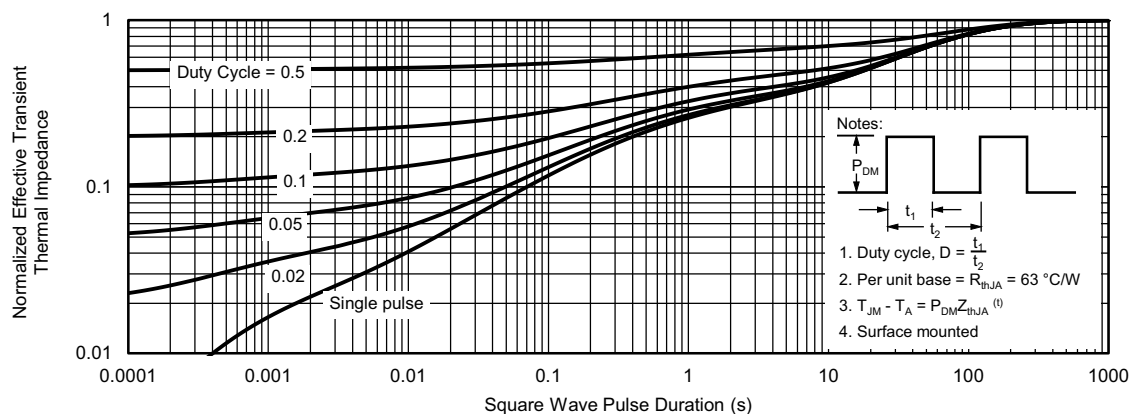
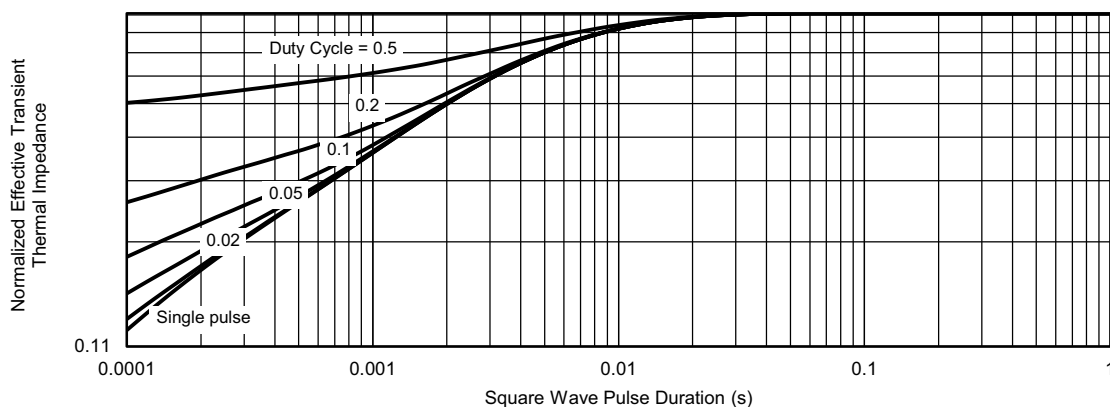


On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

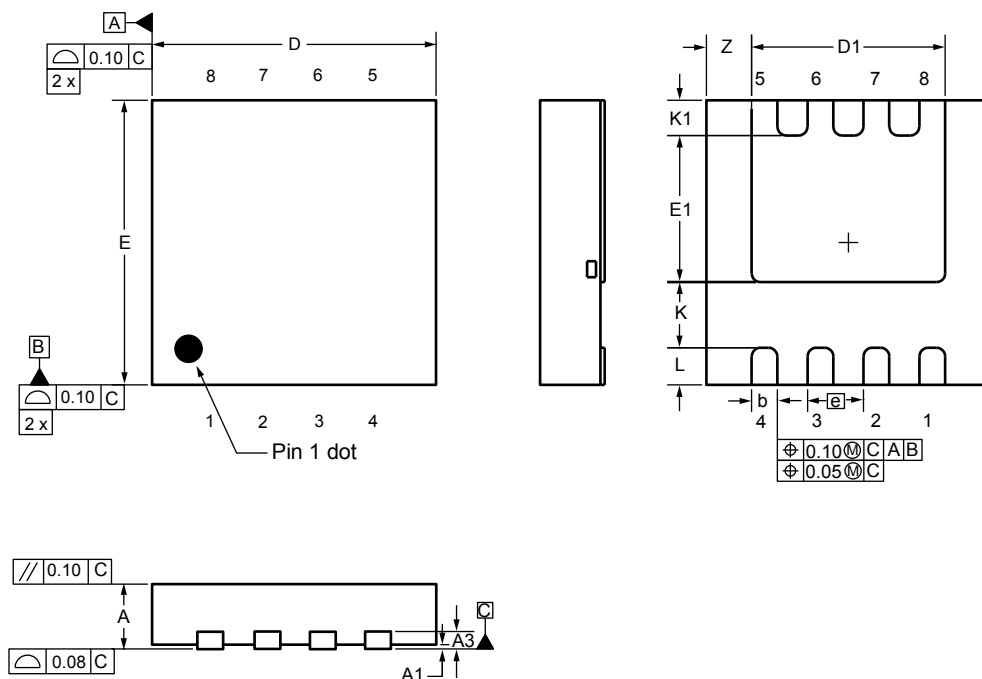
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

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Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: C20-0862-Rev. B, 20-Jul-2020						
DWG: 6008						



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