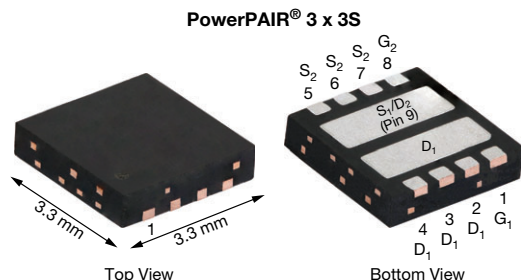


Dual N-Channel 70 V (D-S) MOSFETs



FEATURES

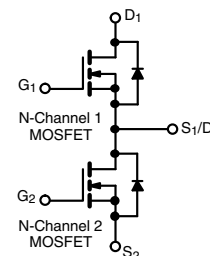
- TrenchFET® Gen IV power MOSFETs
- 100 % R_g and UIS tested
- Integrated MOSFET half bridge power stage
- Optimized Q_{gs}/Q_{gd} ratio improves switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- POL
- Synchronous buck converter
- Telecom DC/DC
- Resonant converters
- Motor drive control



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V_{DS} (V)	70	70
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0161	0.0161
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0209	0.0209
Q_g typ. (nC)	6.1	6.1
I_D (A) ^a	32.5	32.5
Configuration	Dual	

ORDERING INFORMATION	
Package	PowerPAIR 3 x 3S
Lead (Pb)-free and halogen-free	SiZ254DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage		V _{DS}	70	70	V	
Gate-source voltage		V _{GS}	± 20	± 20		
Continuous drain current (T _J = 150 °C)	T _C = 25 °C	I _D	32.5 ^a	32.5 ^a	A	
	T _C = 70 °C		26	26		
	T _A = 25 °C		11.7 ^{b, c}	11.7 ^{b, c}		
	T _A = 70 °C		9.4 ^{b, c}	9.4 ^{b, c}		
Pulsed drain current (100 μs pulse width)		I _{DM}	60	60		
Continuous source drain diode current	T _C = 25 °C	I _S	27	27		
	T _A = 25 °C		3.6 ^{b, c}	3.6 ^{b, c}		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	12	12		
Single pulse avalanche energy		E _{AS}	7.2	7.2	mJ	
Maximum power dissipation	T _C = 25 °C	P _D	33	33	W	
	T _C = 70 °C		21	21		
	T _A = 25 °C		4.3 ^{b, c}	4.3 ^{b, c}		
	T _A = 70 °C		2.8 ^{b, c}	2.8 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^d			260			

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	23	29	23	29	$^\circ\text{C}/\text{W}$
Maximum junction-to-case (drain)	Steady state	R_{thJC}	3	3.8	3	3.8	

Notes

- $T_C = 25^\circ\text{C}$
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR 3 x 3S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is $64^\circ\text{C}/\text{W}$ for channel-1 and $64^\circ\text{C}/\text{W}$ for channel-2



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	Ch-1	70	-	-	V
		V _{GS} = 0 V, I _D = 250 μA	Ch-2	70	-	-	
V _{DS} Temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	Ch-1	-	41	-	mV/°C
		I _D = 10 mA	Ch-2	-	42	-	
V _{GS(th)} Temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	Ch-1	-	-4.9	-	
		I _D = 250 μA	Ch-2	-	-4.9	-	
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.1	-	2.4	V
		V _{DS} = V _{GS} , I _D = 250 μA	Ch-2	1.1	-	2.4	
Gate source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 70 V	Ch-1	-	-	± 100	nA
		V _{DS} = 0 V, V _{GS} = ± 20 V	Ch-2	-	-	± 100	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 70 V, V _{GS} = 0 V	Ch-1	-	-	1	μA
		V _{DS} = 70 V, V _{GS} = 0 V	Ch-2	-	-	1	
		V _{DS} = 70 V, V _{GS} = 0 V, T _J = 55 °C	Ch-1	-	-	5	
		V _{DS} = 70 V, V _{GS} = 0 V, T _J = 55 °C	Ch-2	-	-	5	
On-state drain current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-1	10	-	-	A
		V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-2	10	-	-	
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	Ch-1	-	0.0125	0.0161	Ω
		V _{GS} = 10 V, I _D = 10 A	Ch-2	-	0.0129	0.0161	
		V _{GS} = 4.5 V, I _D = 7 A	Ch-1	-	0.0157	0.0209	
		V _{GS} = 4.5 V, I _D = 7 A	Ch-2	-	0.0159	0.0209	
Forward transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 10 A	Ch-1	-	50	-	S
		V _{DS} = 10 V, I _D = 10 A	Ch-2	-	45	-	
Dynamic ^a							
Input capacitance	C _{iss}	Channel-1 V _{DS} = 35 V, V _{GS} = 0 V, f = 1 MHz Channel-2 V _{DS} = 35 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	-	795	-	pF
Output capacitance	C _{oss}		Ch-2	-	765	-	
			Ch-1	-	125	-	
			Ch-2	-	120	-	
Reverse transfer capacitance	C _{rss}		Ch-1	-	7	-	
			Ch-2	-	7	-	
C _{rss} /C _{iss} ratio			Ch-1	-	-	0.0169	
			Ch-2	-	-	0.0165	
Total gate charge	Q _g	V _{DS} = 35 V, V _{GS} = 10 V, I _D = 10 A	Ch-1	-	13	20	nC
		V _{DS} = 35 V, V _{GS} = 10 V, I _D = 10 A	Ch-2	-	13	20	
		V _{DS} = 35 V, V _{GS} = 4.5 V, I _D = 10 A	Ch-1	-	6.1	9.1	
		V _{DS} = 35 V, V _{GS} = 4.5 V, I _D = 10 A	Ch-2	-	6.1	9.1	
Gate-source charge	Q _{gs}	Channel-1 V _{DS} = 35 V, V _{GS} = 4.5 V, I _D = 10 A	Ch-1	-	2.7	-	
			Ch-2	-	2.5	-	
Gate-drain charge	Q _{gd}	Channel-2 V _{DS} = 35 V, V _{GS} = 4.5 V, I _D = 10 A	Ch-1	-	1.8	-	
			Ch-2	-	1.8	-	
Output charge	Q _{oss}	V _{DS} = 35 V, V _{GS} = 0 V	Ch-1	-	11.5	-	
			Ch-2	-	11.3	-	
Gate resistance	R _g	f = 1 MHz	Ch-1	0.24	1.2	2.4	Ω
			Ch-2	0.2	1	2	

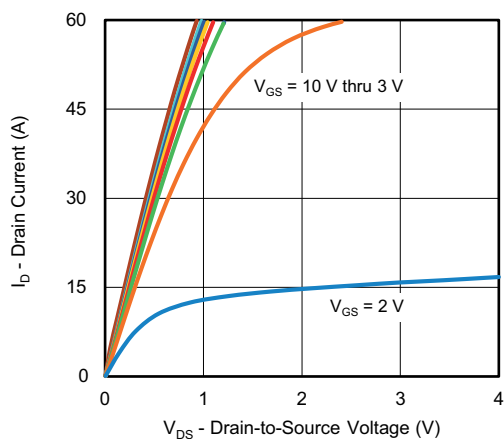
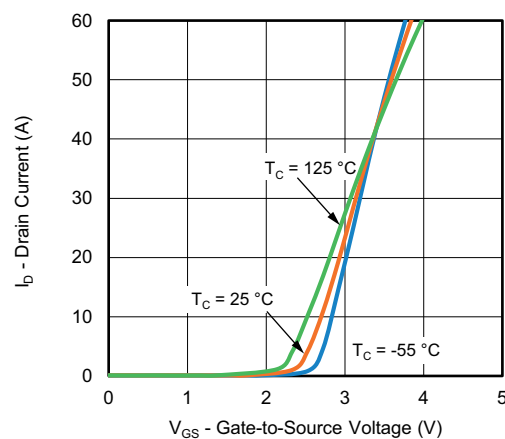
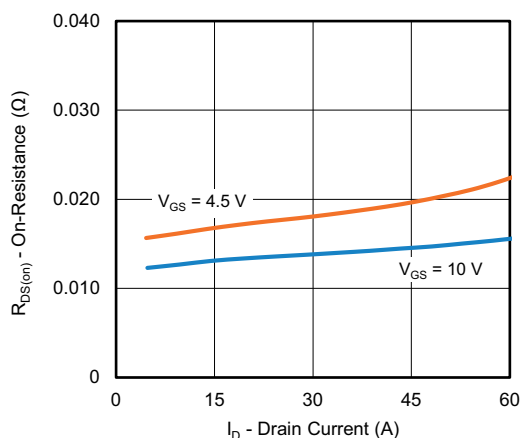
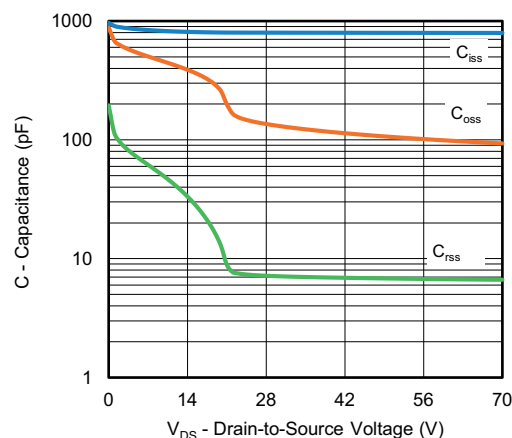
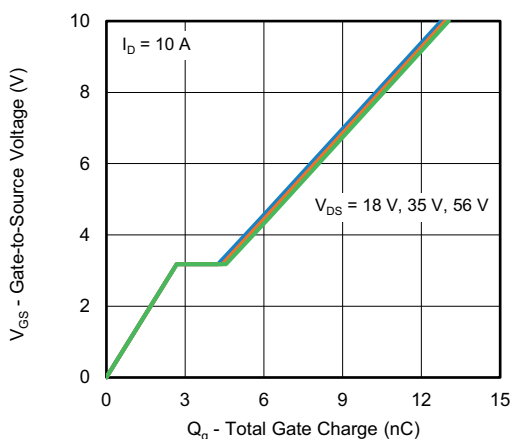
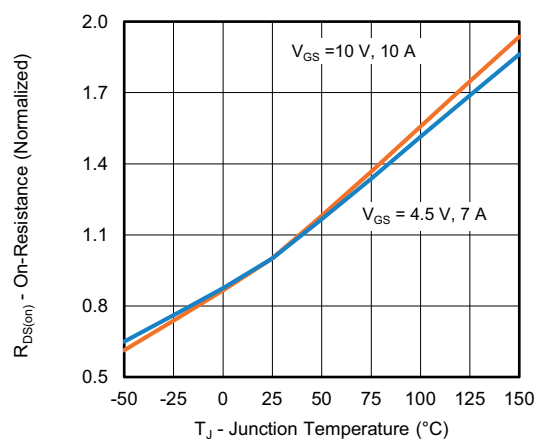


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Dynamic ^a								
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 35 V, R _L = 3 Ω I _D ≡ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	12	24	ns	
			Ch-2	-	12	-		
Rise time	t _r		Ch-1	-	6	12		
			Ch-2	-	6	12		
Turn-off delay time	t _{d(off)}	Channel-2 V _{DD} = 35 V, R _L = 3 Ω I _D ≡ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	24	48		
			Ch-2	-	23	45		
Fall time	t _f		Ch-1	-	6	12		
			Ch-2	-	5	10		
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 35 V, R _L = 3 Ω I _D ≡ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	20	40		
			Ch-2	-	18	36		
Rise time	t _r		Ch-1	-	30	60		
			Ch-2	-	26	52		
Turn-off delay time	t _{d(off)}		Channel-2 V _{DD} = 35 V, R _L = 3 Ω I _D ≡ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	22	44	
				Ch-2	-	22	44	
Fall time	t _f			Ch-1	-	10	20	
				Ch-2	-	10	20	
Drain-Source Body Diode Characteristics								
Continuous source-drain diode current	I _S	T _C = 25 °C	Ch-1	-	-	27	A	
			Ch-2	-	-	27		
Pulse diode forward current (t = 100 μs)	I _{SM}		Ch-1	-	-	60		
			Ch-2	-	-	60		
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	Ch-1	-	0.8	1.2	V	
		I _S = 5 A, V _{GS} = 0 V	Ch-2	-	0.8	1.2		
Body diode reverse recovery time	t _{rr}	Channel-1 I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	22	44	ns	
			Ch-2	-	22	44		
Body diode reverse recovery charge	Q _{rr}			Ch-1	-	21	42	nC
				Ch-2	-	20	40	
Reverse recovery fall time	t _a	Channel-2 I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	17	-	ns	
			Ch-2	-	17	-		
Reverse recovery rise time	t _b			Ch-1	-	5		-
				Ch-2	-	5		-

Notes

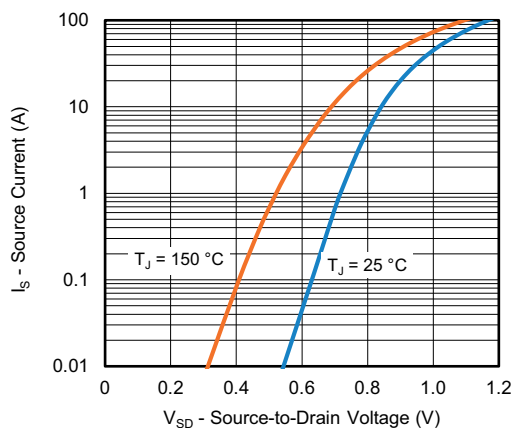
- a. Guaranteed by design, not subject to production testing
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

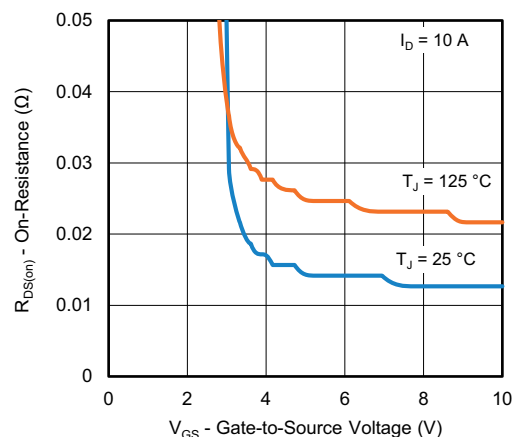
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



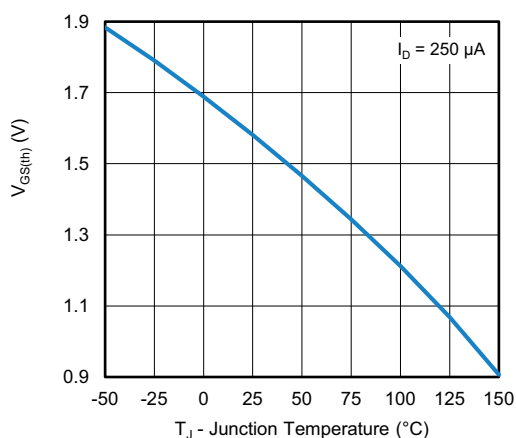
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



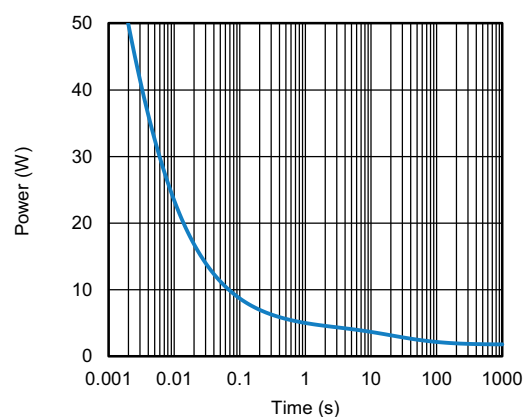
Source-Drain Diode Forward Voltage



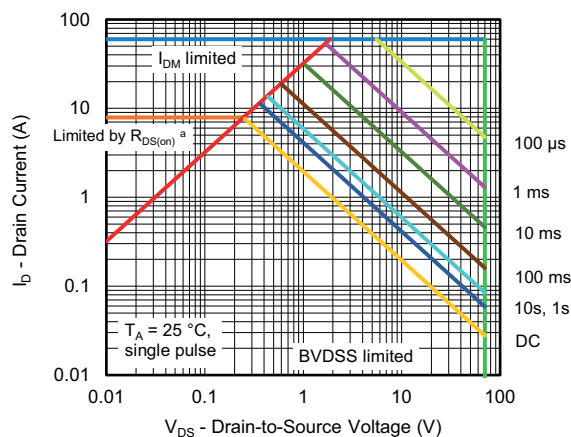
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



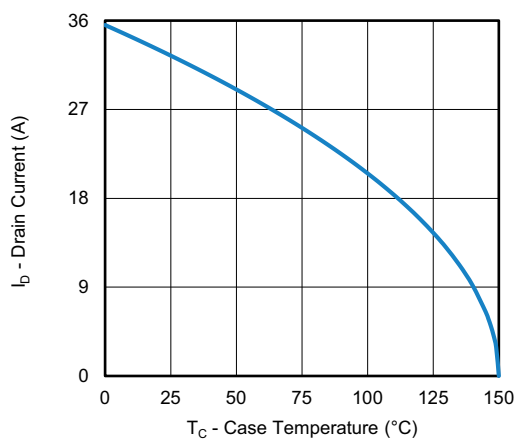
Safe Operating Area, Junction-to-Ambient

Note

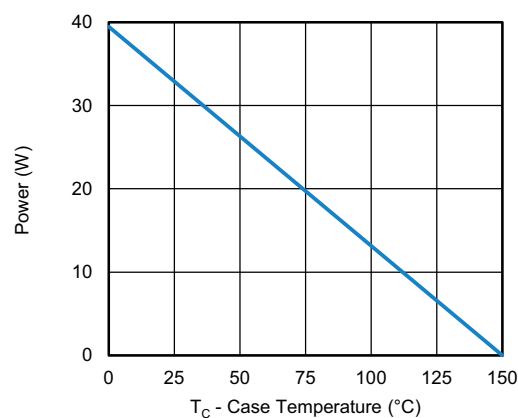
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



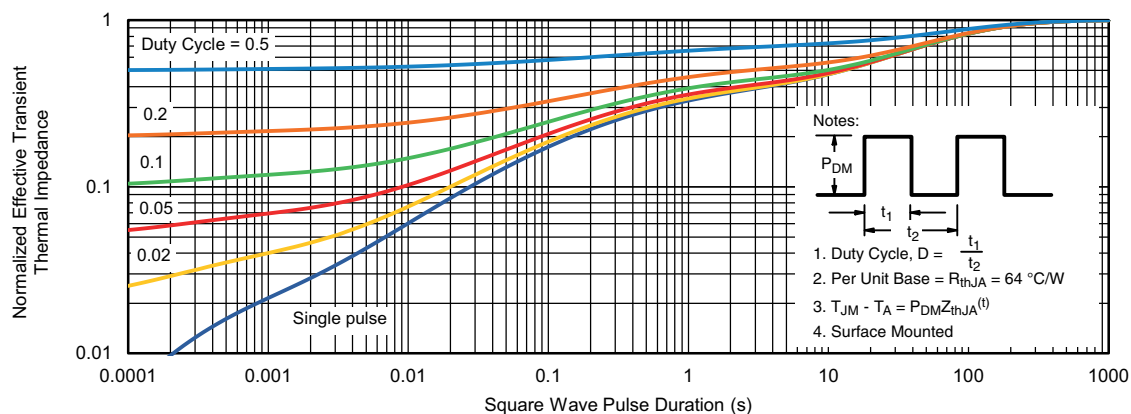
Power, Junction-to-Case

Note

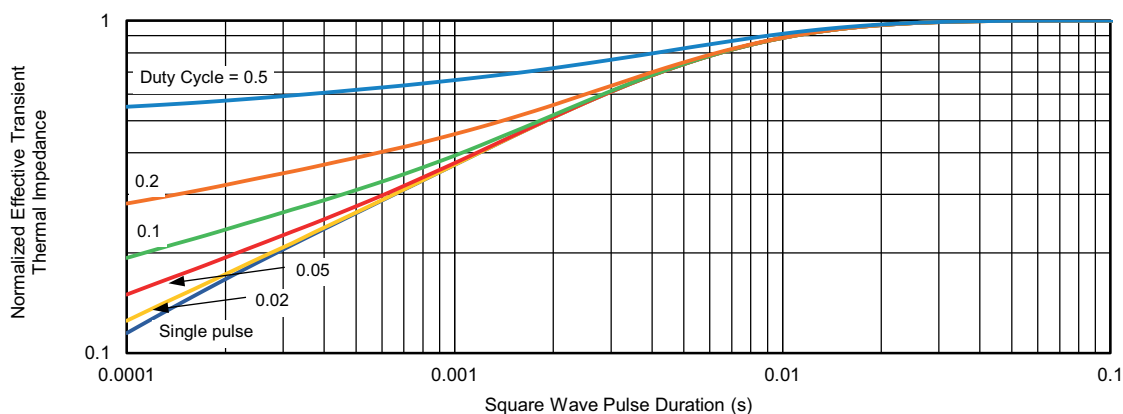
- a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



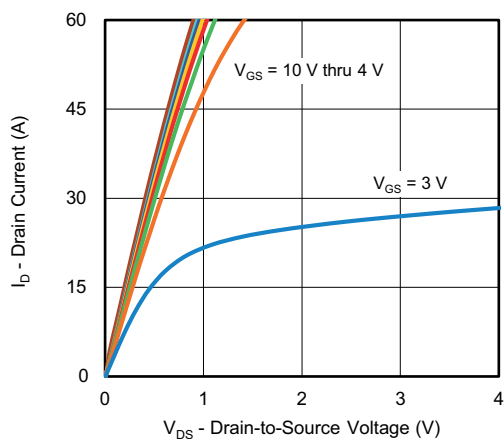
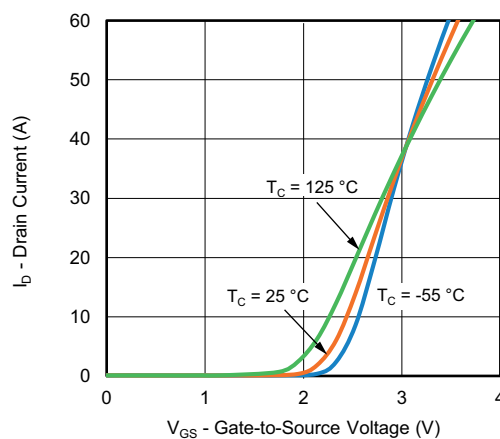
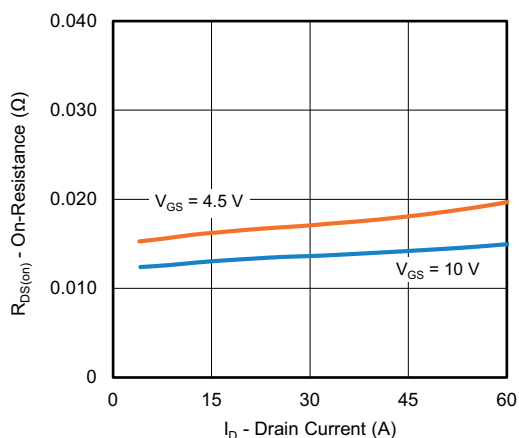
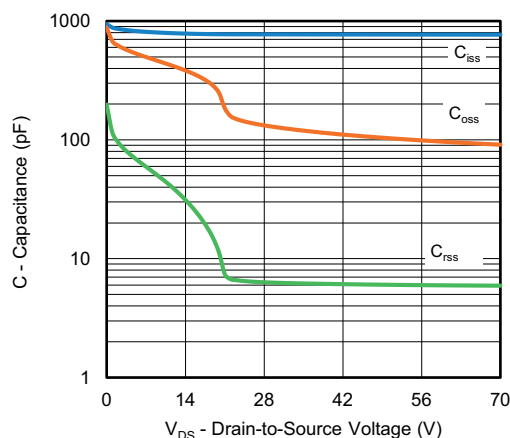
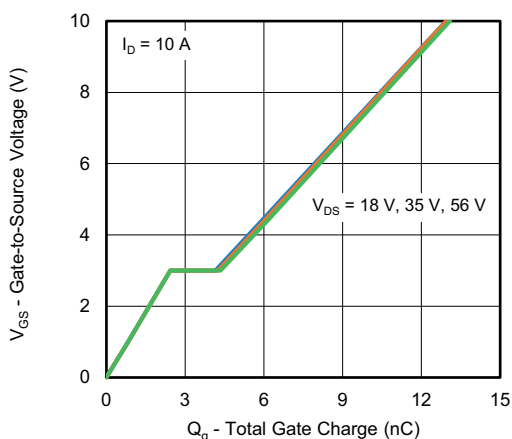
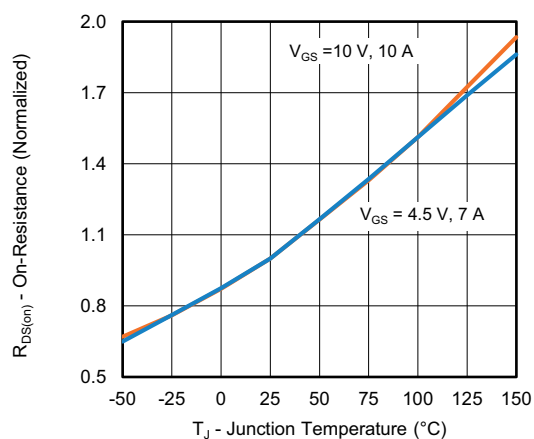
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

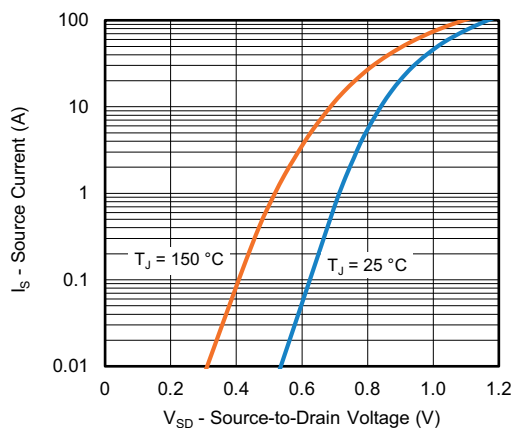


Normalized Thermal Transient Impedance, Junction-to-Case

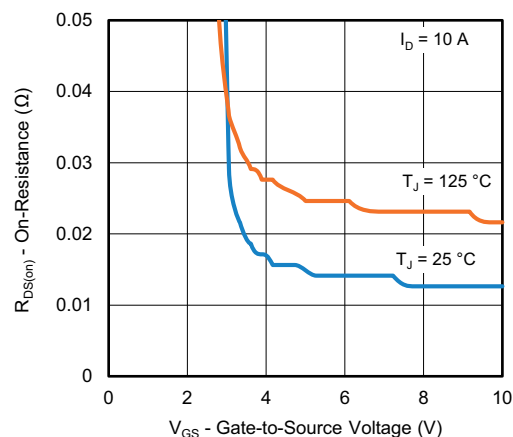
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



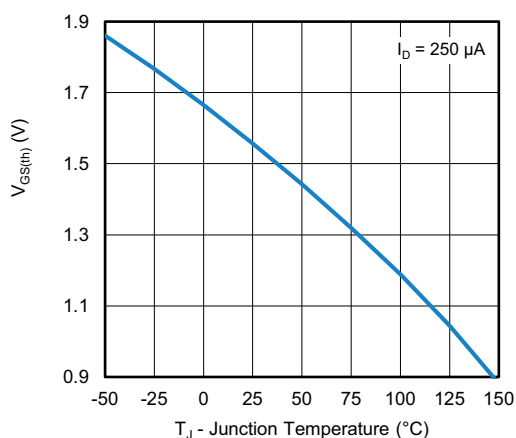
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



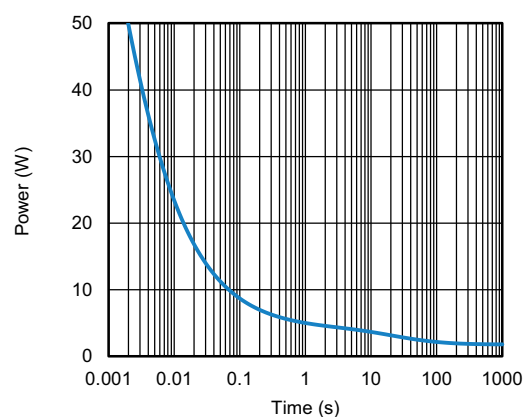
Source-Drain Diode Forward Voltage



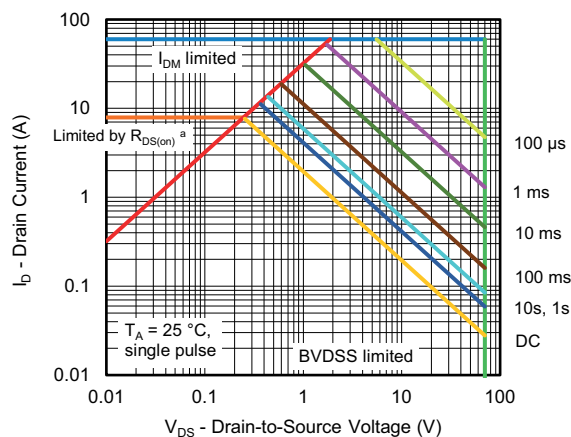
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



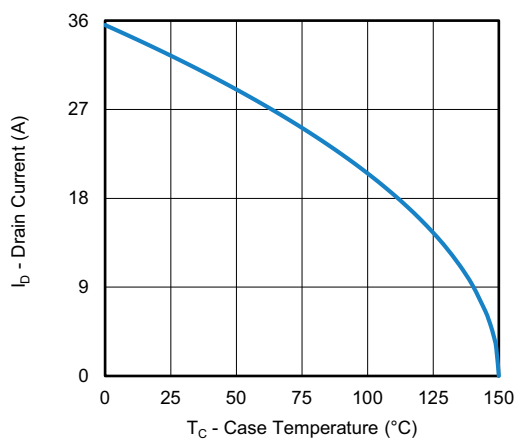
Safe Operating Area, Junction-to-Ambient

Note

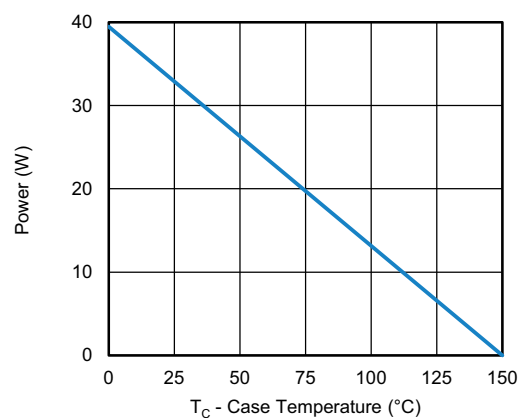
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



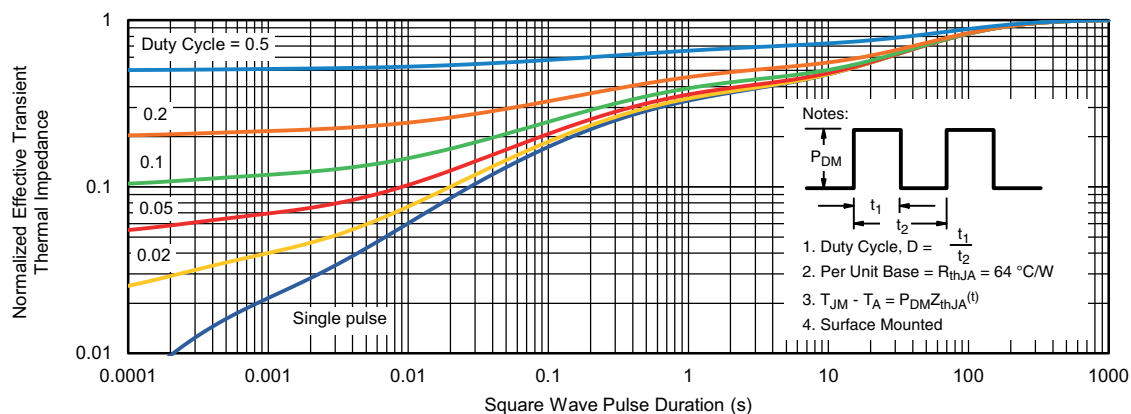
Power, Junction-to-Case

Note

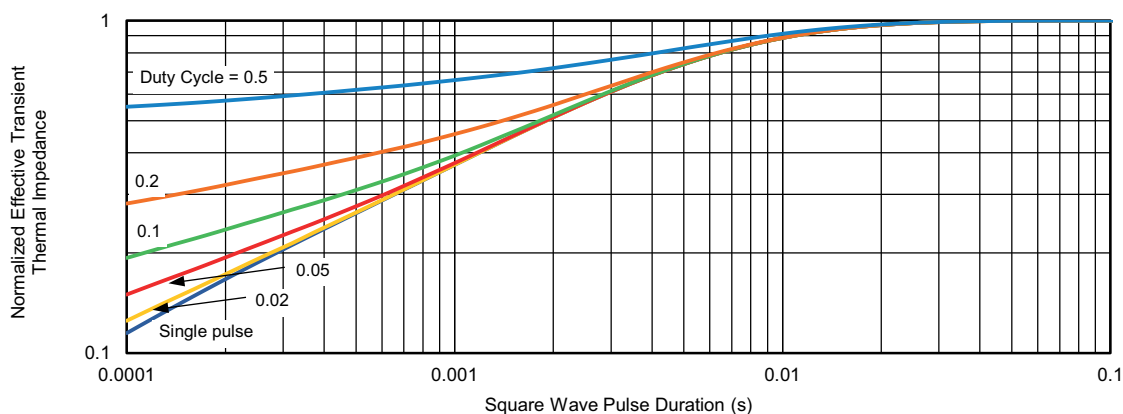
- a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

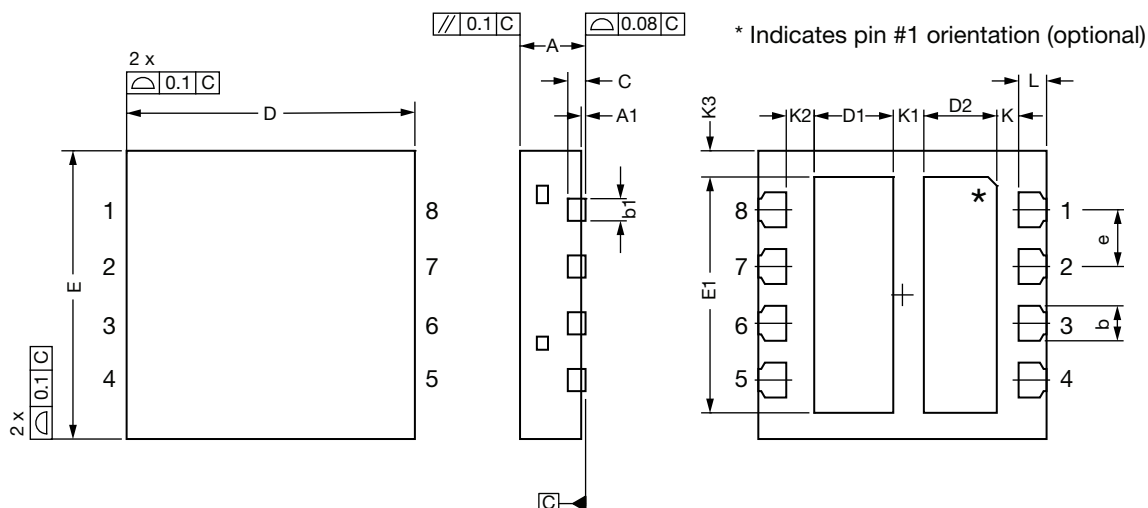


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?79592.



PowerPAIR® 3.3 x 3.3 Case Outline

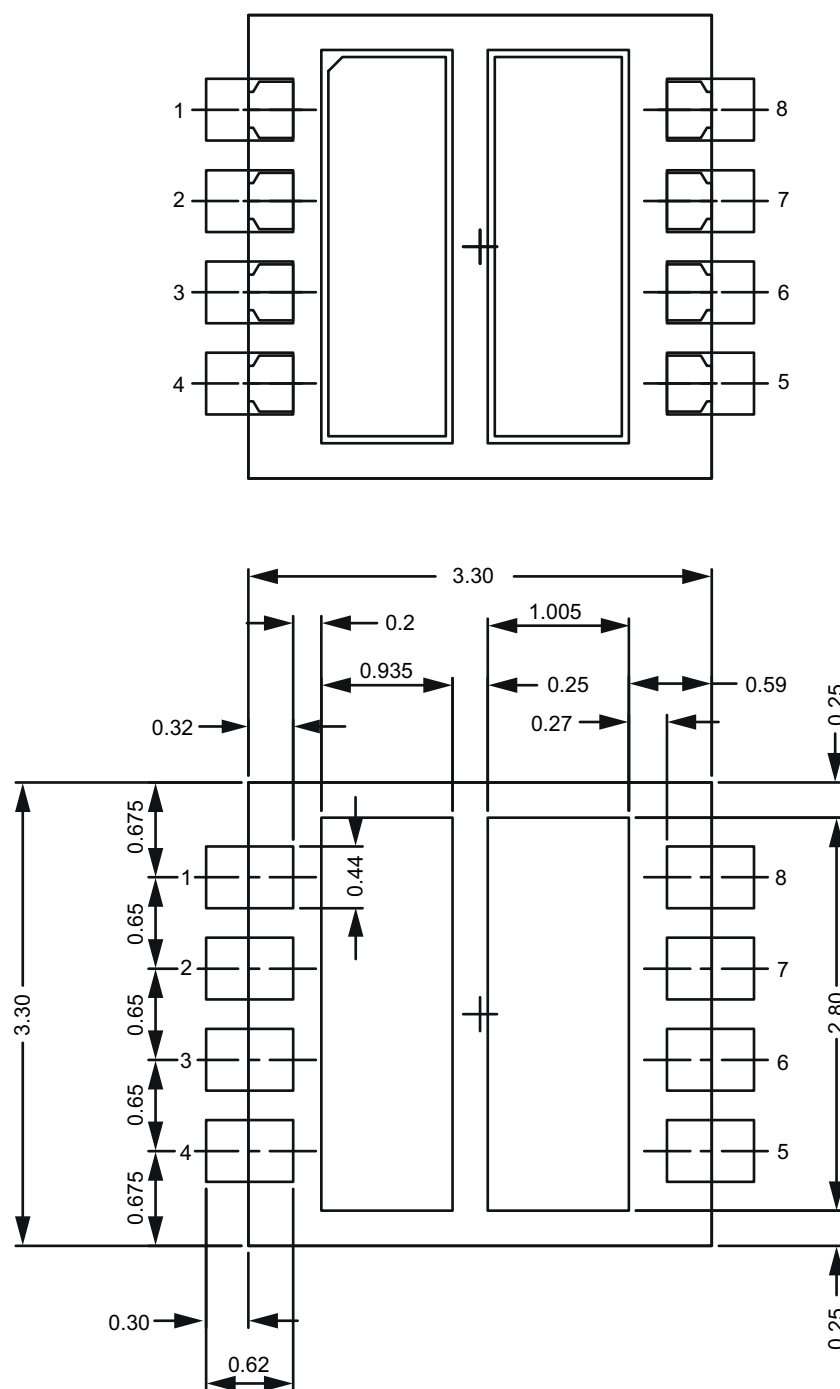


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	0.86	0.91	0.96	0.034	0.036	0.038
D2	0.79	0.84	0.89	0.031	0.033	0.035
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.65	2.70	2.75	0.104	0.106	0.108
e	0.65 BSC			0.026 BSC		
K	0.25 ref.			0.010 ref.		
K1	0.35 ref.			0.014 ref.		
K2	0.32 ref.			0.013 ref.		
K3	0.30 ref.			0.012 ref.		
L	0.27	0.32	0.37	0.011	0.013	0.015
C18-0564-Rev. A, 14-May-2018 DWG: 6066						

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5M - 1994
- (3) N is the number of terminals; Nd is the number of terminals in X-direction; Ne is the number of terminals in Y-direction
- (4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- (5) The pin # 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (6) Exact shape and size of this features is optional
- (7) Package warpage max. 0.08 mm
- (8) Applied only for terminals

Recommended Land Pattern for PowerPAIR® 3 x 3S BWL





Disclaimer

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