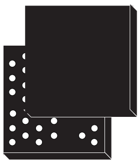
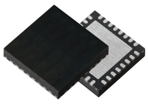
STM32WB05xN

Datasheet

Bluetooth® Low Energy 5.4 certified network coprocessor



WLCSP36 (2.652 mm x 2.592 mm)



VFQFPN32 (5 x 5 mm)

Product status	
STM32WB05xN	STM32WB05KN STM32WB05TN

Features

Includes ST state-of-the-art patented technology.

Bluetooth® Low Energy network coprocessor supporting the Bluetooth 5.4 specifications

- 2 Mbps data rate
- Long range (Coded PHY)
- Advertising extensions
- Direction finding (AoA/AoD)
- LE ping procedure
- Periodic advertising and periodic advertising sync transfer

Radio

- RX sensitivity level: -97 dBm @ 1 Mbps, -104 dBm @ 125 kbps (long range)
- Programmable output power up to +8 dBm (at antenna connector)
- Data rate supported: 2 Mbps, 1 Mbps, 500 kbps and 125 kbps
- Integrated balun
- Support for external PA and LNA
- Available integrated passive device (IPD) companion chip for optimized matching and filtering

Ultra-low-power radio performance

- 8 nA in Shutdown mode (1.8 V)
- 0.8 µA in Deepstop mode (with external LSE and Bluetooth LE wake-up sources, 1.8 V)
- 1.0 µA in Deepstop mode (with internal LSI and Bluetooth LE wake-up sources, 1.8 V)
- 4.3 mA peak current in TX (@ 0 dBm, 3.3 V)
- 3.4 mA peak current in RX (@ sensitivity level, 3.3 V)

High performance and ultra-low-power Arm® Cortex®-M0+ 32-bit, running up to 64 MHz

Dynamic current consumption: 14 µA/MHz

Operating supply voltage: from 1.7 to 3.6 V

-40 °C to 105 °C temperature range

Supply and reset management

- High efficiency embedded SMPS step-down converter with intelligent bypass mode
- Ultra-low-power power-on-reset (POR) and power-down-reset (PDR)
- Programmable voltage detector (PVD)

Clock sources

- 64 MHz PLL

- Fail safe 32 MHz crystal oscillator with integrated trimming capacitors
- 32 kHz crystal oscillator
- Internal low-power 32 kHz RO

System peripherals

- 1x DMA controller with 8 channels supporting SPI-I2S, USART
- 1x SPI
- 1x USART

Up to 20 fast I/Os

- All of them with wake-up capability
- All of them retain state in low-power
- All of them 5 V tolerant

Development support

- Serial wire debug (SWD)

All packages are ECOPACK2 compliant.

Applications

- Industrial
- Home and industrial automation
- Asset tracking, ID location, real-time locating system
- Smart lighting
- Fitness,wellness and sports
- Healthcare, consumer medical
- Security/proximity
- Remote control
- Assisted living
- Mobile phone peripherals
- PC peripherals

1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WB05xN microcontrollers, based on Arm® core.

For information on the Arm® Cortex®-M0+ core, refer to the Cortex®-M0+ technical reference manual, available from the www.arm.com website.

For information on Bluetooth® refer to www.bluetooth.com website.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32WB05xN is an ultra-low-power Bluetooth® Low Energy wireless network coprocessor addressing standard Bluetooth® LE protocol. Interface with external micro controller can be achieved through SPI and USART. It embeds STMicroelectronics’s state-of-the-art 2.4 GHz radio IPs, optimized for ultra-low-power consumption and excellent radio performance, for unparalleled battery lifetime. It is compliant with Bluetooth Low Energy SIG core specification version 5.4.

The STM32WB05xN embeds a Arm® Cortex®-M0+ microcontroller that can operate up to 64 MHz and also the BlueNRG core co-processor (DMA based) for Bluetooth Low Energy timing critical operations.

The STM32WB05xN features standard and advanced communication interfaces:

- 1x SPI
- 1x USART

The STM32WB05xN operates in the -40 to +105 °C temperature range from a 1.7 V to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The STM32WB05xN integrates a high efficiency SMPS step-down converter and an integrated PDR circuitry with a fixed threshold that generates a device reset when the V_{DD} drops under 1.65 V.

The STM32WB05xN comes in different package versions supporting up to:

- 20 I/Os for the VFQFPN32 package
- 20 I/Os for the WLCSP36 package

Table 1. STM32WB05xx device features and peripheral counts

Feature		STM32WB05KN	STM32WB05TN
Bluetooth Low Energy		Yes	
Communication interfaces	SPI	1	
	USART	1	
Wake-up pins		20	
GPIOs		20	
Maximum CPU frequency		64 MHz	
Operating temperature		-40 °C to 105 °C temperature range	
Operating voltage		1.7 to 3.6 V	
Package		VFQFPN32 5 x 5 mm, 0.50 mm pitch, very fine pitch quad flat no lead package	WLCSP36 2.652 x 2.592 mm, 0.40 mm pitch, wafer level chip scale array package

3 Functional overview

3.1 Arm Cortex-M0+ core with MPU

The STM32WB05xN contains an Arm Cortex-M0+ microcontroller core. The Arm Cortex-M0+ was developed to provide a low-cost platform that meets the needs of CPU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. The Arm Cortex-M0+ can run from 1 MHz up to 64 MHz.

The Arm Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The interrupts are handled by the Arm Cortex-M0+ Nested Vector Interrupt Controller (NVIC). The NVIC controls specific Arm Cortex-M0+ interrupts as well as the STM32WB05xN peripheral interrupts. With its embedded ARM core, the STM32WB05xN family is compatible with all Arm tools and software.

3.2 RF subsystem

The STM32WB05xN embeds an ultra-low-power radio, compliant with Bluetooth® Low Energy (Bluetooth® LE) specification. The Bluetooth® LE features 1 Mbps and 2 Mbps transfer rates as well as long range options (125 kbps, 500 kbps), supports multiple roles simultaneously acting at the same time as Bluetooth® Low Energy sensor and hub device.

The Bluetooth® LE protocol stack is implemented by an efficient system partitioned as follows:

- Hardware part: BlueCore handling time critical and time consuming Bluetooth® LE protocol parts
- Firmware part: Arm® Cortex-M0+ core handling non time critical Bluetooth® LE protocol parts

3.2.1 RF front-end block diagram

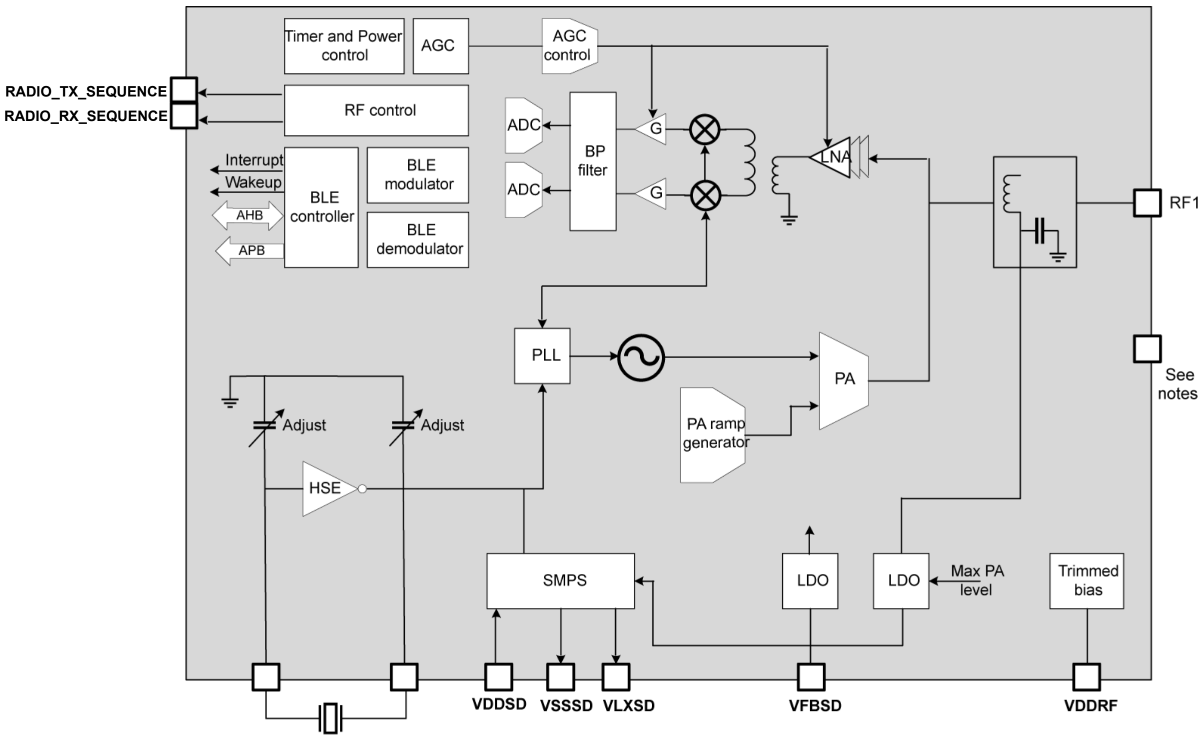
The RF front end is based on a direct modulation of the carrier in TX, and uses a low IF architecture in RX mode.

Thanks to an internal transformer with RF pins, the circuit directly interfaces the antenna (single ended connection, impedance close to 50 Ω). The natural band pass behavior of the internal transformer simplifies outside circuitry aimed at harmonic filtering and out of band interferer rejection.

In transmit mode, the maximum output power is user selectable through the programmable LDO voltage of the power amplifier. A linearized, smoothed analog control offers a clean power ramp-up.

In receive mode the circuit can be used in standard high performance or in reduced power consumption (user programmable). The automatic gain control (AGC) is able to reduce the chain gain at both RF and IF locations, for an optimized interferer rejection. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity, and excellent linearity can be achieved.

Figure 1. STM32WB05xN RF block diagram



Note: VFQFPN32: VSS through exposed pad,and VSSRF pins must be connected to the ground plane.
WLCSP36: VSSRF pins must be connected to the ground plane.

3.2.2 IPDs for STM32WB05xN

Table 2 lists the available IPD variants for the STM32WB05xN device.

Table 2. IPDs for STM32WB05xN

IPD	MCU Package	STM32WB05xN part number
MLPF-NRG-01D3	VFQFPN32	STM32WB05KN
	WLCSP36	STM32WB05TN

3.3 Power supply management

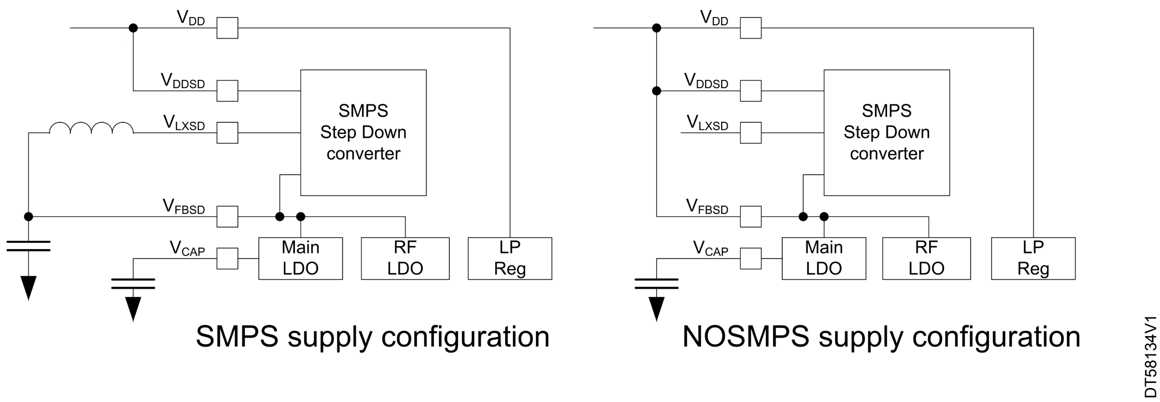
3.3.1 SMPS step-down regulator

The device integrates a step-down converter to improve low power performance when the V_{DD} voltage is high enough. The SMPS output voltage can be programmed from 1.2 V to 1.90 V. It is internally clocked at 4 MHz or 8 MHz.

The device can be operated without the SMPS by just wiring its output to VDD. This is the case for applications where the voltage is low, or where the power consumption is not critical.

Except for the configuration SMPS OFF, an L/C BOM must be present on the board and connected to the VFBSD pad.

Figure 2. Power supply configuration



3.3.2 Power supply schemes

The STM32WB05xN embeds three power domains:

- V_{DD33} (V_{DDIO} or V_{DD}):
  - the voltage range is between 1.7 V and 3.6 V
  - it supplies a part of the I/O ring, the embedded regulators and the system analog IPs as power management block and embedded oscillators
- V_{DD12o}:
  - always-on digital power domain
  - this domain is generally supplied at 1.2 V during active phase of the device
  - this domain is supplied at 1.0 V during low power mode (Deepstop)
- V_{DD12i}:
  - interruptible digital power domain
  - this domain is generally supplied at 1.2 V during active phase of the device
  - this domain is shut down during low power mode (Deepstop)

3.3.3 Linear voltage regulators

The digital power supplies are provided by different regulators:

- The main LDO (MLDO):
  - it provides 1.2 V from a 1.4-3.3 V input voltage
  - it supplies both V_{DD12i} and V_{DD12o} when the device is active
  - it is disabled during the low power mode (Deepstop)

- Low power LDO (LPREG):
  - it stays enabled during both active and low power phases
  - it provides 1.0 V voltage
  - it is not connected to the digital domain when the device is active
  - it is connected to the V_{DD12o} domain during low power mode (Deepstop)
- A dedicated LDO (RFLDO) to provide a 1.2 V to the analog RF block

An embedded SMPS step-down converter is available (inserted between the external power and the LDOs).

3.3.4 Power supply supervisor

The STM32WB05xN device embeds several power voltage monitoring:

- Power-on-reset (POR): during the power-on, the device remains in reset mode if V_{DDIO} is below a V_{POR} threshold (typically 1.65 V)
- Power-down-reset (PDR): during power-down, the PDR puts the device under reset when the supply voltage (V_{DD}) drops below the V_{PDR} threshold (around 20 mV below V_{POR}). The PDR feature is always enabled
- Programmable voltage detector (PVD): can be used to monitor the V_{DDIO} (against a programmed threshold) or an external analog input signal. When the feature is enabled and the PVD measures a voltage below the comparator, an interrupt is generated (if unmasked)

3.4 Reset management

The STM32WB05xN offers two different resets:

- The PORESETn: this reset is provided by the low power management unit (LPMU) analog block and corresponds to a POR or PDR root cause. It is linked to power voltage ramp-up or ramp-down. This reset impacts all resources of the . The exit from Shutdown mode is equivalent to a POR and thus generates a PORESETn. The PORESETn signal is active when the power supply of the device is below a threshold value or when the regulator does not provide the target voltage.
- The PADRESETn (system reset): this reset is built through several sources:
  - PORESETn
  - Reset due to the watchdog
    The STM32WB05xN device embeds a watchdog timer, which may be used to recover from software crashes
  - Reset due to CPU Lockup
    The Cortex-M0+ generates a lockup to indicate the core is in the lock-up state resulting from an unrecoverable exception. The lock-up reset is masked if a debugger is connected to the Cortex-M0+
  - Software system reset
    The system reset request is generated by the debug circuitry of the Cortex-M0+. The debugger sets the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR). This system reset request through the AIRCR can also be done by the embedded software (into the hardfault handler for instance)
  - Reset from the RSTN external pin
    The RSTN pin toggles to inform that a reset has occurred

  This PADRESETn resets all resources of the STM32WB05xN, except:
  - Debug features
  - Power controller unit

The pulse generator guarantees a minimum reset pulse duration of 20 μs for each internal reset source. In case of reset from the RSTN external pad, the reset pulse is generated when the pad is asserted low.

3.5 Operating modes

Several operating modes are defined for the STM32WB05xN:

- Run mode
- Deepstop mode
- Shutdown mode

Table 3. **Relationship between the low power modes and functional blocks**

Mode	Shutdown	Deepstop	IDLE	Run
CPU	OFF	OFF	OFF	ON
Radio	OFF	OFF	ON/OFF	ON/OFF
Supply system	OFF	OFF	ON (DC-DC ON/OFF)	ON (DC-DC ON/OFF)
Register retention	OFF	ON	ON	ON
HS clock	OFF	OFF	ON	ON
LS clock	OFF	ON/OFF	ON	ON
Peripherals	OFF	OFF	ON/OFF	ON/OFF
Wake on GPIOs	OFF	ON/OFF	ON/OFF	NA
Wake on reset pin	ON	ON	ON	NA
GPIOs configuration retention	PWRC pull-up/pull-down only	ON	ON	ON

3.5.1 Run mode

In Run mode the STM32WB05xN is fully operational:

- All interfaces are active
- The internal power supplies are active
- The system clock and the bus clock are running
- The CPU core and the radio can be used

The power consumption may be reduced by gating the clock of the unused peripherals.

3.5.2 Deepstop mode

Deepstop is the only low-power mode of the STM32WB05xN allowing the restart from a saved context environment and the application at wake-up to go on running.

The conditions to enter Deepstop mode are:

- The radio is sleeping (no radio activity)
- The CPU is sleeping (WFI with SLEEPDEEP bit activated)
- No unmasked wake-up sources are active
- The low-power mode selection (LPMS) bit of the power controller unit is 0 (default)
- The GPIO Retention Mode Selection (GPIORET) bit of the Power Controller unit must be set

In Deepstop mode:

- The system and the bus clocks are stopped
- Only the essential digital power domain is ON and supplied at 1.0 V
- The I/Os pull-up and pull-down can be controlled during Deepstop mode, depending on the software configuration
- The low speed clock can be running or stopped, depending on the software configuration:
  - ON or OFF
  - Sourced by LSE or by LSI
- The radio wake-up block, including its timer, stay active (if enabled and the low speed clock is ON)
- Up to 20 GPIOs retaining their configuration:
  - I/Os retain the Run mode configuration while in Deepstop mode
- Up to 20 I/Os are able to be in output driving:
  - A static low or high level
- Some I/Os are able to be in output driving:
  - The low speed clock (on PA10)

Possible wake-up sources are:

- The radio block is able to generate two events to wake up the system through its embedded wake-up timer running on low speed clock:
  - Radio wake-up time is reached
  - CPU host wake-up time is reached
- All GPIOs are able to wake up the system

At wake-up, all the hardware resources located in the digital power domain that are OFF during the Deepstop mode, are reset. The CPU reboots. The wake-up reason is visible in the register of the power controller.

3.5.3 Shutdown mode

The Shutdown mode is the least power consuming mode.

The conditions to enter Shutdown mode are the same conditions needed to enter Deepstop mode except that the LPMS bit of the power controller unit is 1.

In Shutdown mode, the STM32WB05xN is in ultra-low-power consumption: all voltage regulators, clocks and the RF interface are not powered. The STM32WB05xN can enter shutdown mode by internal software sequence. The only way to exit shutdown mode is by asserting and deasserting the RSTN pin.

In Shutdown mode:

- The system is powered down as both the regulators are OFF
- The V_{DDIO} power domain is ON
- All the clocks are OFF, LSI and LSE are OFF
- The I/Os pull-up and pull-down can be controlled during Shutdown mode, depending on the software configuration
- The only wake-up source is a low pulse on the RSTN pin

The exit from Shutdown is similar to a POR startup. The PDR feature can be enabled or disabled during Shutdown.

3.6 Clock management

Three different clock sources may be used to drive the system clock of the STM32WB05xN:

- HSI: high speed internal 64 MHz RC oscillator
- PLL64M: 64 MHz PLL clock
- HSE: high speed 32 MHz external crystal

The STM32WB05xN also has a low speed clock tree used by some timers in the radio.

Three different clock sources can be used for this low speed clock tree:

- Low speed internal (LSI): low speed and low drift internal RC with a fixed frequency between 24 kHz and 49 kHz depending on the sample
- Low speed external (LSE) from:
  - An external crystal 32.768 kHz
  - A single-ended 32.738 kHz input signal
- A 32 kHz clock derived from dividing HSI or HSE. In this case, the slow clock is not available in Deepstop low-power mode

By default, after a system reset, all low speed sources are OFF.

Both the activation and the selection of the slow clock are relevant during Deepstop mode and at wake-up as slow clock generates a clock for the timers involved in wake-up event generation.

The HSI and the PLL64M clocks are provided by the same analog block called RC64MPLL. The 64 MHz clock output by this block can be:

- A nonaccurate clock when no external XO provides an input clock to this block (HSI)
- An accurate clock when the external XO provides the 32 MHz and once its internal PLL is locked (PLL64M)

The following clocks are used:

- USART: it uses an always 16 MHz clock to have a fixed reference clock for baud rate management. The goal is to allow the CPU to boost or slow down the system clock (depending on on-going activities) without impacting a potential on-going serial interface transfer on external I/Os
- SPI: the baud rate is managed by the system clock. This implies its baud rate is impacted by dynamic system clock frequency changes.

- Radio: it does not directly use the system clock for its APB/AHB interfaces, but the system clock with a potential divider (1 or 2 or 4). In parallel, the radio uses an always 16 MHz and an always 32 MHz for modulator, demodulator and to have a fixed reference clock to manage specific delays

3.7 General purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB0 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access (DMA)

The DMA is used in order to provide high-speed data transfer between peripherals and memory as well as memory-to-memory. Data can be quickly moved by DMA without any CPU actions. In this manner, CPU resources are free for other operations.

The DMA controller has eight channels in total. Each has an arbiter to handle the priority among DMA requests.

DMA main features are:

- Eight independently configurable channels (requests)
- Each of the eight channels is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software
- Priorities among requests from channels of DMA are software programmable (four levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, and so on)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer (RAM only)
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to SRAMs, APB0 and APB1 peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

3.9 Nested vectored interrupt controller (NVIC)

The interrupts are handled by the Cortex-M0+ nested vector interrupt controller (NVIC). NVIC controls specific Cortex-M0+ interrupts as well as the STM32WB05xN peripheral interrupts.

The NVIC benefits are the following:

- Nested vectored interrupt controller that is an integral part of the ARM Cortex-M0+
- Tightly coupled interrupt controller provides low interrupt latency
- Control system exceptions and peripheral interrupts
- NVIC supports 32 vectored interrupts
- Four programmable interrupt priority levels with hardware priority level masking
- Software interrupt generation using the ARM exceptions SVCall and PendSV
- Support for NMI
- ARM Cortex M0+ vector table offset register VTOR implemented

NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.10 Universal synchronous/asynchronous receiver transmitter (USART)

USART offers flexible full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. USART is able to communicate with a speed up to 2 Mbit/s. Furthermore, USART is able to detect and automatically set its own baud rate, based on the reception of a single character.

High speed data communication is possible by using DMA (direct memory access) for multibuffer configuration.

3.11 Serial peripheral interface (SPI)

The STM32WB05xN has one SPI interface (SPI3) allowing communication up to 32 Mbit/s in both master and slave modes. The SPI peripheral supports:

- Master or slave operation
- Multimaster support
- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- Serial communication with external devices
- NSS management by hardware or software for both master and slave: dynamic change of master/slave operations
- SPI Motorola support
- SPI TI mode support
- Hardware CRC feature for reliable communication

All SPI interfaces can be served by the DMA controller.

3.12 Serial wire debug port

The STM32WB05xN embeds an ARM SWD interface that allows interactive debugging and programming of the device. The interface is composed of only two pins: DEBUG_SWDIO and DEBUG_SWCLK. The enhanced debugging features for developers allow up to 4 breakpoints and up to 2 watchpoints.

3.13 TX and RX event alert

The STM32WB05xN is provided with the RADIO_TX_SEQUENCE and RADIO_RX_SEQUENCE signals which alert, respectively, transmission and reception activities.

A signal can be enabled for TX and RX on two pins, through alternate functions:

- RADIO_TX_SEQUENCE is available on PA10 (AF2) or PB14 (AF1).
- RADIO_RX_SEQUENCE is available on PA8 (AF2) or PA11 (AF2).

The signal is high when radio is in TX (or RX), low otherwise.

The signals can be used to control external antenna switching and support coexistence with other wireless technologies.

Note: The RADIO_RF_ACTIVITY signal is used to notify if there is an ongoing RF operation (either TX or RX). It is a logical OR between the RADIO_RX_SEQUENCE and RADIO_TX_SEQUENCE. This signal can be used to enable an antenna switch component when achieving antenna switching during AoA or AoD operation.

3.14 Direction finding

The STM32WB05xN Bluetooth® radio controller supports the angle of arrival (AoA) and angle of departure (AoD) features by managing:

- the constant tone extension (CTE) inside a packet
- the antenna switching mechanism for both AoA and AoD.

The antenna switching mechanism provides a 7-bit antenna identifier RADIO_ANTENNA_ID[6:0] indicating the antenna number to be used.

In a AoD transmitter or in a AoA receiver, the radio needs to switch antenna during the CTE field of the packet. For this purpose, the RADIO_ANTENNA_ID signal can be enabled on some I/Os, by programming them in the associated alternate function. This signal needs to be provided to an external antenna switching circuit, since RADIO_ANTENNA_ID[0] is the least significant bit and ANTENNA _ID[6] the most significant bit of the antenna identifier to be used.

4 Pinouts and pin description

The STM32WB05xN comes in two package versions: WLCSP36 offering 20 GPIOs and VFQFPN32 offering 20 GPIOs.

Figure 3. Pinout top view (VFQFPN32 package)

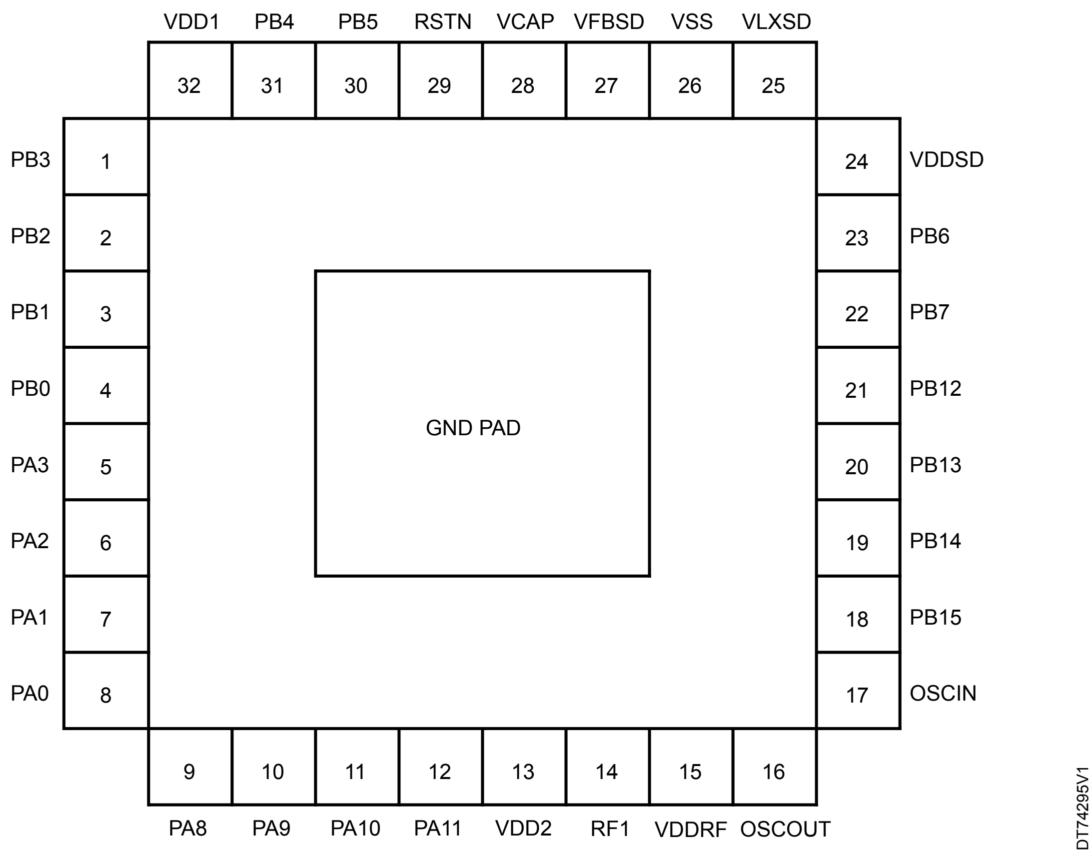


Figure 4. Pinout bump side view (WLCSP36 package)

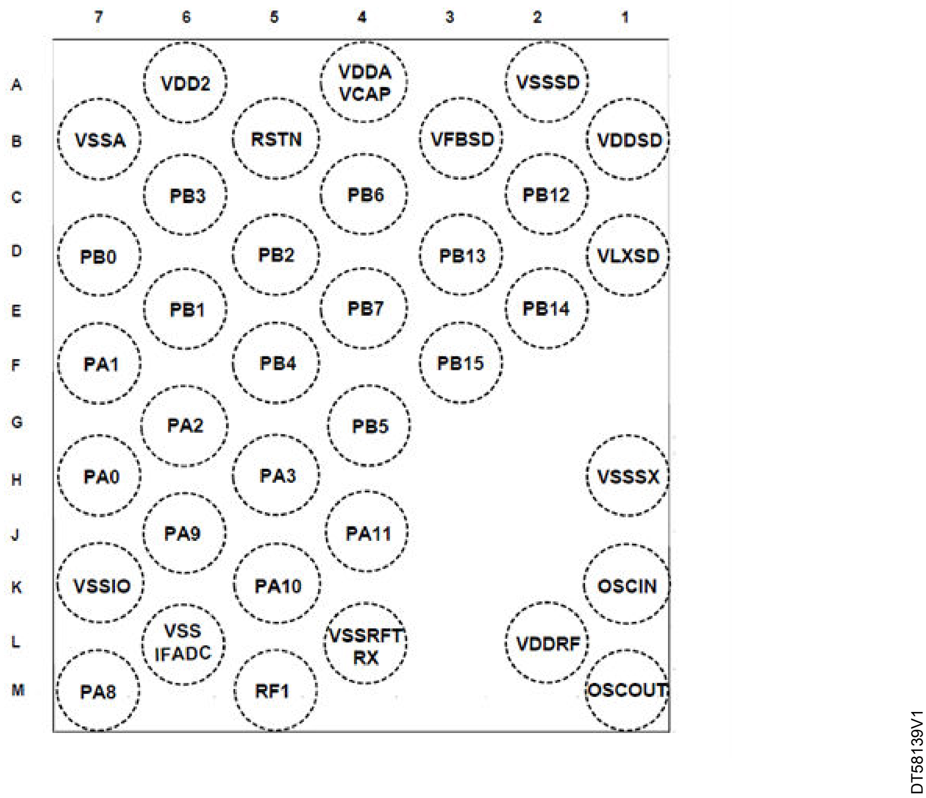


Table 4. Pin descriptions

Pin number		Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
VFQFPN32	WLCSP36					
1	C6	PB3	I/O	FT_a	USART_CTS, SPI3_SCK, RADIO_ANTENNA_ID[3]	PWR_WKUP3
2	D5	PB2	I/O	FT_a	USART_RTS_DE, RADIO_ANTENNA_ID[2]	PWR_WKUP2
3	E6	PB1	I/O	FT_a	USART_CK, RADIO_ANTENNA_ID[1]	PWR_WKUP1
4	D7	PB0	I/O	FT_a	USART_RX, RADIO_ANTENNA_ID[0]	PWR_WKUP0
5	H5	PA3	I/O	FT_a	DEBUG_SWCLK, USART_RTS_DE, SPI3_SCK	PWR_WKUP15
6	G6	PA2	I/O	FT_a	DEBUG_SWDIO, USART_CK	PWR_WKUP14
7	F7	PA1	I/O	FT_f	USART_TX	PWR_WKUP13
8	H7	PA0	I/O	FT_f	USART_CTS	PWR_WKUP12
9	M7	PA8	I/O	FT	USART_RX, RADIO_RX_SEQUENCE, SPI3_MISO	PWR_WKUP8, RTC_OUT
10	J6	PA9	I/O	FT	USART_TX, RTC_OUT, SPI3_NSS	PWR_WKUP9
11	K5	PA10	I/O	FT	RADIO_TX_SEQUENCE, I2S3_MCK	PWR_WKUP10
12	J4	PA11	I/O	FT	RADIO_RX_SEQUENCE, SPI3_MOSI	PWR_WKUP11
13	A6	VDD2	S	-	-	1.7-3.6 battery voltage input
14	M5	RF1	I/O	RF	-	RF input/output. Impedance 50 Ω
15	L2	VDDRF	S	-	-	1.7-3.6 battery voltage input
16	M1	OSCOUT	I/O	FT_a	-	32 MHz crystal
17	K1	OSCIN	I/O	FT_a	-	32 MHz crystal
18	F3	PB15	I/O	FT_a	USART_TX	PWR_WKUP19
19	E2	PB14	I/O	FT_a	RADIO_TX_SEQUENCE, USART_RX	PWR_PVD_IN, PWR_WKUP18
20	D3	PB13	I/O	FT_a	-	PWR_WKUP17
21	C2	PB12	I/O	FT_a	-	PWR_WKUP16
22	E4	PB7	I/O	FT_f	USART_CTS, RADIO_RF_ACTIVITY	PWR_WKUP7
23	C4	PB6	I/O	FT_f	RADIO_ANTENNA_ID[6]	PWR_WKUP6
24	B1	VDDSD	S	-	-	1.7-3.6 battery voltage input
25	D1	VLXSD	S	-	-	SMPS input/output
26	A2	VSSSD	S	-	-	SMPS Ground
27	B3	VFBSD	S	-	-	SMPS output
28	A4	VDDA_ VCAP	S	-	-	1.2 V digital core
29	B5	RSTN	I/O	RST	-	Reset pin
30	G4	PB5	I/O	FT_a	RADIO_ANTENNA_ID[5]	PWR_WKUP5
31	F5	PB4	I/O	FT_a	RADIO_ANTENNA_ID[4]	PWR_WKUP4
32	-	VDD1	S	-	-	1.7-3.6 battery voltage input

Pin number		Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
VFQFPN32	WLCSP36					
-	B7	VSSA	S	-	-	-
-	k7	VSSIO	S	-	-	Ground I/O
-	L6	VSSIFADC	S	-	-	Ground analog RF
-	H1	VSSSX	S	-	-	Ground analog RF
-	L4	VSSRFTRX	S	-	-	Ground analog RF
Exposed pad	-	GND	S	-	-	Ground

Table 5. **Legend/abbreviations used in the pinout table**

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below, the pin name and the pin function during and after reset are the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Options for TT or FT I/Os	
		_f(1).	I/O, Fm+ capable
		_a(2).	I/O, with analog switch function supplied by IO BOOSTER(3)
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. *The related I/O structures in Section 4: Pinouts and pin description are: FT_f*
2. *The related I/O structures in Section 4: Pinouts and pin description are: FT_a*
3. *IO BOOSTER block allows the good behavior of those switches to be guaranteed when the VBAT goes below 2.7 V.*

Table 6. **Alternate function port A**

Port		AF0	AF1	AF2	AF3	AF5	AF7
		SYS_AF/USART	USART	RTC USART/RF	SPI3	SYS_AF	SYS_AF
Port A	PA0	-	USART_CTS	-	-	-	-
	PA1	-	-	USART_TX	-	-	-
	PA2	DEBUG_SWDIO	USART_CK	-	-	DEBUG_SWDIO	DEBUG_SWDIO
	PA3	DEBUG_SWCLK	USART_RTS_DE	-	SPI3_SCK	DEBUG_SWCLK	DEBUG_SWCLK
	PA8	USART_RX	-	RADIO_RX_ SEQUENCE	SPI3_MISO	-	-
	PA9	USART_TX	-	RTC_OUT	SPI3_NSS	-	-
	PA10	-	-	RADIO_TX_ SEQUENCE	-	-	-
	PA11	-	-	RADIO_RX_ SEQUENCE	SPI3_MOSI	-	-

Table 7. **Alternate function port B**

Port		AF0	AF1	AF2	AF3	AF4	AF6	AF7
		USART	SYS_AF	-	TIM2/SYS_AF	SPI3	RF/USART	-
Port B	PB0	USART_RX	-	-	-	-	RADIO_ANTENNA_ID[0]	-
	PB1	USART_CK	-	-	-	-	RADIO_ANTENNA_ID[1]	-
	PB2	USART_RTS_DE	-	-	-	-	RADIO_ANTENNA_ID[2]	-
	PB3	USART_CTS	-	-	-	SPI3_SCK	RADIO_ANTENNA_ID[3]	-
	PB4	-	-	-	-	-	RADIO_ANTENNA_ID[4]	-
	PB5	-	-	-	-	-	RADIO_ANTENNA_ID[5]	-
	PB6	-	-	-	-	-	RADIO_ANTENNA_ID[6]	-
	PB7	-	-	USART_CTS	-	-	RADIO_RF_ACTIVITY	-
	PB12	-	-	-	-	-	-	-
	PB13	-	-	-	-	-	-	-
	PB14	-	RADIO_TX_SEQUENCE	-	-	-	USART_RX	-
	PB15	-	-	-	-	-	USART_TX	-

5 Application circuits

The schematics below are purely indicative.

Figure 5. Application circuit: DC-DC converter, WLCSP36 package

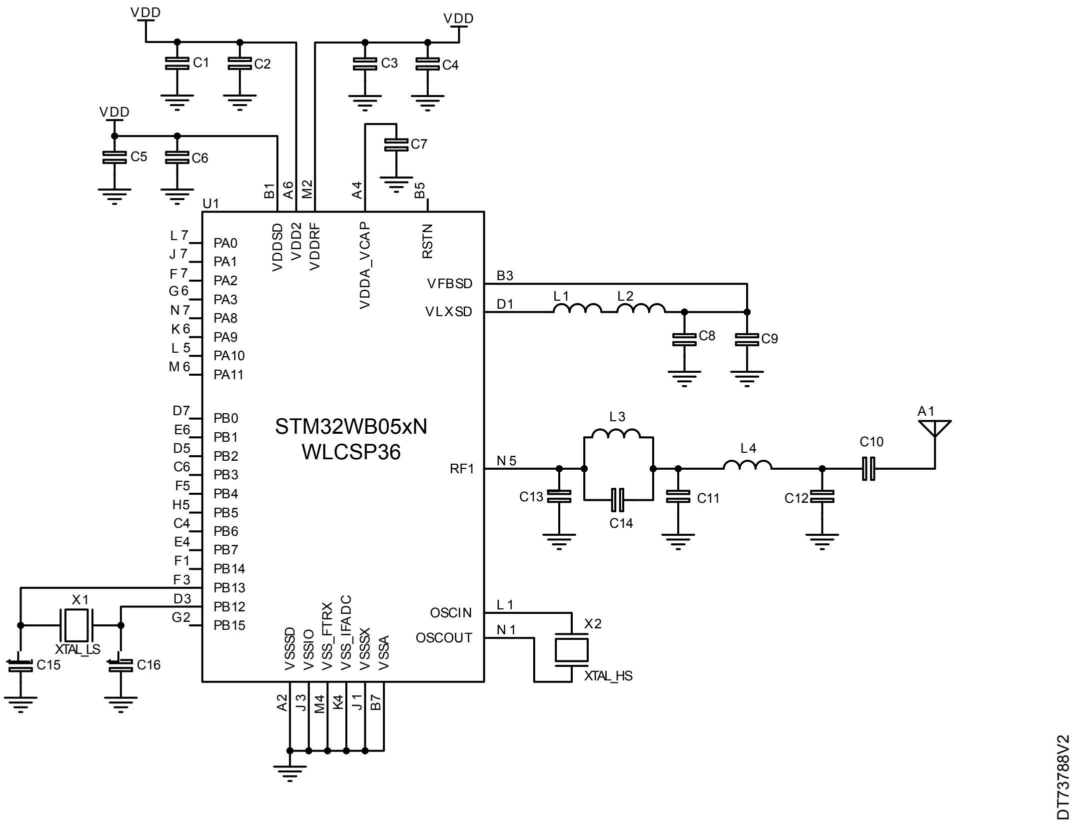


Figure 6. Application circuit: DC-DC converter, VFQFPN32 package

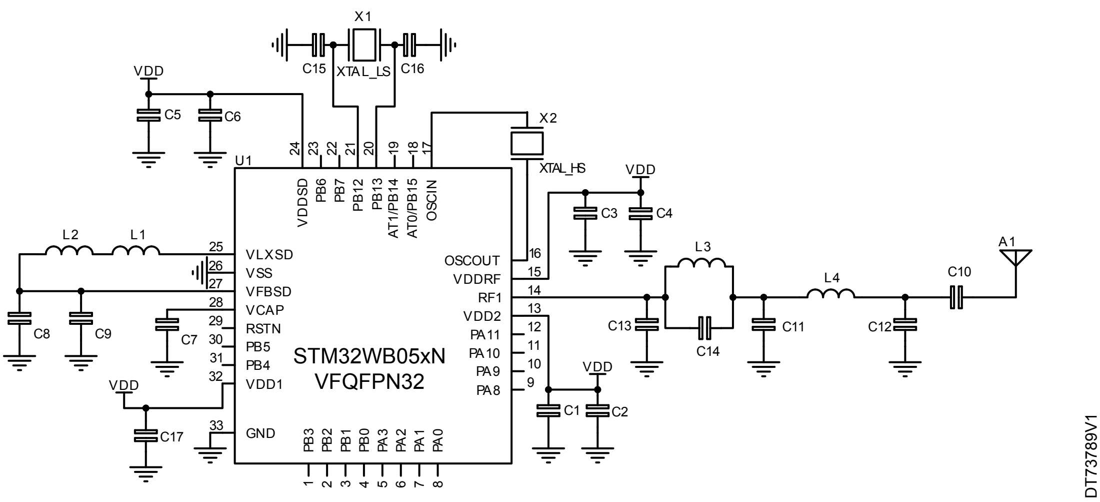


Table 8. Application circuit external components

Component	Description
C1	Decoupling capacitor
C2	Decoupling capacitor
C3	Decoupling capacitor
C4	Decoupling capacitor
C5	Decoupling capacitor
C6	Decoupling capacitor
C7	Main LDO capacitor
C8	DC–DC converter output capacitor
C9	DC–DC converter output capacitor
C10	DC block capacitor
C11	RF matching capacitor
C12	RF Matching capacitor
C13	RF Matching capacitor
C14	RF Matching capacitor
C15	32 kHz crystal loading capacitor
C16	32 kHz crystal loading capacitor
C17	Decoupling capacitor
L1	DC-DC converter output inductor
L2	DC-DC converter noise filter
L3	RF matching inductor
L4	RF matching inductor
X1	Low speed crystal
X2	High speed crystal
U1	STM32WB05xN

Note: In order to make the board DC–DC OFF, the inductance L1 must be removed and the supply voltage must be applied to the VFBSD pin.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to ground (GND).

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the following standard conditions:

- Ambient temperature is T_A = 25 °C
- Supply voltage is V_{DD}: 3.3 V
- System clock frequency is 32 MHz (clock source HSI)
- SMPS clock frequency is 4 MHz

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V. They are given only as design guidelines and are not tested.

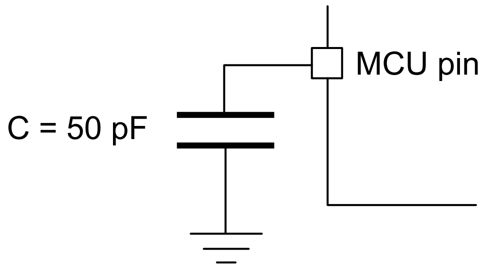
6.1.3 Typical curves

Unless otherwise specified, all typical curves are only given as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

Figure 7. Pin loading conditions

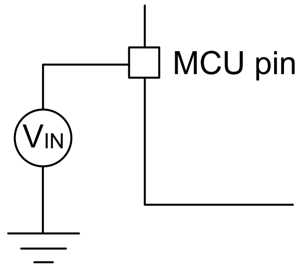


DT57473V1

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure below.

Figure 8. Pin input voltage



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6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DDRF}, V_{DDSD}	DC-DC converter supply voltage input and output	-0.3	+3.9	V
V_{DDA_VCAP}	DC voltage on linear voltage regulator	-0.3	+1.32	
FXTALOUT, FXTALIN	DC Voltage on HSE	-0.3	1.32	
PA0 to PA15, PB0 to PB15	DC voltage on digital input/output pins	-0.3	+3.9	
V_{LXSD}, V_{FBSD}	DC voltage on analog pins			
PB12, PB13	DC voltage on crystal pins	-0.3	+3.6	
RF1	DC voltage on RF pin		+1.4	-
$\|\Delta V_{DD}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV

Note: All the main power and ground pins must always be connected to the external power supply, in the permitted range.

Table 10. Current characteristics

Symbol	Ratings	Max.	Unit
ΣIV_{DD}	Total current into sum of all VDD power lines (source)	130	mA
ΣIV_{GND}	Total current out of sum of all ground lines (sink)	130	
$IV_{DD(PIN)}$	Maximum current into each VDD power pin (source)	100	
$IV_{GND(PIN)}$	Maximum current out of each ground pin (sink)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins	100	
	Total output current sourced by sum of all I/Os and control pins	100	
$\Sigma\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)	-5/0	

Table 11. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-40 to -125	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

6.3.1 Summary of main performance

Table 12. Main performance SMPS ON

Symbol	Parameter	Test conditions	Typ. V_{DD} = 1.8 V	Typ. V_{DD} = 3.3 V	Unit
I_{CORE}	Core current consumption	Shutdown	8	19	nA
		Deepstop, no timer, wake-up GPIO, all RAM retained	0.63	0.64	µA
		Deepstop (32 kHz LSI), all RAMs retained	1.09	1.15	
		Deepstop (32 kHz LSE), all RAM retained	0.88	0.99	
		CPU in Run (64 MHz). Dhrystone, clock source PLL64	-	2638	µA
		CPU in Run (32 MHz). Dhrystone, clock source PLL64	-	2186	
		CPU in WFI (64 MHz), all peripherals off, clock source PLL64	-	1688	
		CPU in WFI (16 MHz), all peripherals off, clock source Direct HSE	-	1000	
		Radio RX at sensitivity level	-	3350	
		Radio TX 0 dBm output power	-	4300	
		Radio RX at sensitivity level with CPU in WFI (32 MHz), clock source Direct HSE	-	4950	
		Radio TX 0 dBm output power with CPU in WFI (32 MHz), clock source Direct HSE	-	5600	
$I_{DYNAMIC}$	Dynamic current	Computed value: (CPU 64 MHz Dhrystone - CPU 32 MHz Dhrystone) / 32	-	14	µA/MHz

Table 13. Main performance SMPS bypassed

Symbol	Parameter	Test conditions	Typ. V_{DD} = 1.8 V	Typ. V_{DD} = 3.3 V	Unit
I_{CORE}	Core current consumption	Shutdown	8	19	nA
		Deepstop, no timer, wake-up GPIO, all RAM retained	0.63	0.64	µA
		Deepstop (32 kHz LSI), all RAMs retained	1.09	1.15	
		Deepstop (32 kHz LSE), all RAM retained	0.88	0.99	
		CPU in Run (64 MHz). Dhrystone, clock source PLL64	-	4450	
		CPU in WFI (64 MHz), all peripherals off, clock source PLL64	-	2313	
		CPU in WFI (16 MHz), all peripherals off, clock source Direct HSE	-	700	
		Radio RX at sensitivity level	-	6700	
		Radio TX 0 dBm output power	-	8900	
		Radio RX at sensitivity level with CPU in WFI (32MHz), clock source Direct HSE	-	9200	
		Radio TX 0 dBm output power with CPU in WFI (32MHz), clock source Direct HSE	-	11000	

Table 14. Peripheral current consumption at V_{DD} = 3.3 V, system clock (CLK_SYS), SMPS on

Parameter	Test conditions	Typ.	Unit
DMA	-	37	µA
GPIOA	-	2	
GPIOB	-	2	
SPI3	-	46	
USART	-	79	
SYSCFG	-	22	

6.3.2 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	1	64	MHz
f_{PCLK0}	Internal APB0 clock	-	1	64	
f_{PCLK1}	Internal APB1 clock frequency	-	1(1)	64	
f_{PCLK2}	Internal APB2 clock frequency	-	16	32	
V_{DD}	Standard operating voltage	-	1.7	3.6	V
V_{FBSMPS}	SMPS feedback voltage	-	1.4	3.6	
V_{DDRF}	Minimum RF voltage	-	1.7	3.6	
V_{IN}	I/O input voltage	-	-0.3	V_{DD}+0.3	
P_D	Power dissipation at T_A=105 °C(2)	VFQFPN32 package	-	30	mW
T_A	Ambient temperature	Maximum power dissipation	-40	105	°C
T_J	Junction temperature range	-	-40	105	

1. *It could be 0 if all the peripherals are disabled.*
2. *T_A cannot exceed T_J max.*

6.3.3 RF general characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 16. Bluetooth Low Energy RF general characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{RANGE}	Frequency range(1)	-	2400	-	2483.5	MHz
RF_{CH}	RF channel center frequency(1)	-	2402	-	2480	MHz
PLL_{RES}	RF channel spacing(1)	-	-	2	-	MHz
ΔF	Frequency deviation(1)	-	-	250	-	kHz
Δf1	Frequency deviation average(1)	-	450	-	550	kHz
C_{Fdev}	Center frequency deviation(1)	During the packet and including both initial frequency offset and drift	-	-	±150	kHz
Δfa	Frequency deviation Δf2 (average) / Δf1 (average)(1)	-	0.80	-	-	-
R_{gfsk}	On-air data rate(1)	-	1	-	2	Mbps
STacc	Symbol time accuracy(1)	-	-	-	±50	ppm
MOD	Modulation scheme	-	GFSK			-
BT	Bandwidth-bit period product	-	-	0.5	-	-
Mindex	Modulation index(1)	-	0.45	0.5	0.55	-
PMAX	Maximum output	At antenna connector, VSMPS = 1.9 V, LDO code	-	+8	-	dBm
PMIN	Minimum output	At antenna connector	-	-20	-	dBm
PRFC	RF power accuracy	@ 27 °C	-	±1.5	-	dB
		All temperatures	-	±2.5	-	

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

6.3.4 RF transmitter characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 17. Bluetooth Low Energy RF transmitter characteristics at 1 Mbps not coded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW1M}	6 dB bandwidth for modulated carrier	Using resolution bandwidth of 100 kHz	500	-	-	kHz
P_{RF1}, 1 Ms/s	In-band emission at ±2 MHz(1)	Using resolution bandwidth of 100 kHz and average detector	-	-46	-	dBm
P_{RF2}, 1 Ms/s	In-band emission at ±[3+n]MHz, where n=0,1,2..(1)	Using resolution bandwidth of 100 kHz and average detector	-	-46	-	dBm
PS_{PUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector	-	-	-41	dBm
$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=2,3,4..k	-50	-	+50	kHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #1 – integration interval #0	-23	-	+23	kHz
$Int_{Freqdrift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-5), where n=6,7,8..k	-20	-	+20	kHz
Drift Rate max	Maximum drift rate(1)	Between any two 10-bit groups separated by 50 µs	-20	-	+20	kHz/50 µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Z_{RF1}	Optimum RF load (impedance at RF1 pin)	@ 2440 MHz	-	40	-	Ω

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

Table 18. Bluetooth Low Energy RF transmitter characteristics at 2 Mbps not coded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW1M}	6 dB bandwidth for modulated carrier	Using resolution bandwidth of 100 kHz	670	-	-	kHz
P_{RF1}, 2 Ms/s	In-band emission at ±4 MHz(1)	Using resolution bandwidth of 100 kHz and average detector	-	-47	-	dBm
P_{RF2}, 2 Ms/s	In-band emission at±5 MHz(1)	Using resolution bandwidth of 100 kHz and average detector	-	-47	-	dBm
P_{RF3}, 2 Ms/s	In-band emission at ±[6+n]MHz, where n=0,1,2..(1)	Using resolution bandwidth of 100 kHz and average detector	-	-51	-	dBm
P_{SPUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector	-	-	-41	dBm
$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=2,3,4..k	-50	-	+50	kHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #1 – integration interval #0	-23	-	+23	kHz
$IntFreq_{drift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-5), where n=6,7,8..k	-20	-	+20	kHz
$DriftRate_{max}$	Maximum drift rate(1)	Between any two 20-bit groups separated by 50 µs	-20	-	+20	kHz/50µs
Z_{RF1}	Optimum RF load (impedance at RF1 pin)	@ 2440 MHz	-	40	-	Ω

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

Table 19. Bluetooth Low Energy RF transmitter characteristics at 1 Mbps LE coded (S=8)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW}	6 dB bandwidth for modulated carrier	Using resolution bandwidth of 100 kHz	500	-	-	kHz
$P_{RF1,\ LE}$ coded	In-band emission at ±2 MHz(1)	Using resolution bandwidth of 100 kHz and average detector	-	-46	-	dBm
$P_{RF2,\ LE}$ coded	In-band emission at ±[3+n] MHz, where n=0,1,2..(1)	Using resolution bandwidth of 100 kHz and average detector	-	-46	-	dBm
PS_{PUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector	-	-	-41	dBm
$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=1,2,3..k	-50	-	+50	kHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #3 – integration interval #0	-19.2	-	+19.2	kHz
$IntFreq_{drift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-3), where n=7,8,9..k	-19.2	-	+19.2	kHz
$DriftRate_{max}$	Maximum drift rate(1)	Between any two 16-bit groups separated by 48 µs	-19.2	-	+19.2	kHz/48 µs
Z_{RF1}	Optimum RF load (Impedance at RF1 pin)	@ 2440 MHz	-	40	-	Ω

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

6.3.5 RF receiver characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 20. Bluetooth Low Energy RF receiver characteristics at 1 Msym/s uncoded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-97	-	dBm
P_{SAT}	Saturation	PER < 30.8%	-	8	-	dBm
Z_{RF1}	Optimum RF source (impedance at RF1 pin)	@ 2440 MHz	-	40	-	Ω
RF selectivity with Bluetooth LE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal = -67 dBm, PER < 30.8%	-	8	-	dBc
$C/I_{1\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz	Wanted signal = -67 dBm, PER < 30.8%	-	-1	-	dBc
$C/I_{2\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -67 dBm, PER < 30.8%	-	-35	-	dBc
$C/I_{3\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal = -67 dBm, PER < 30.8%	-	-47	-	dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image}$	Wanted signal = -67 dBm, PER < 30.8%	-	-25	-	dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal= -67 dBm, PER < 30.8%	-	-25	-	dBc
Out of band blocking (interfering signal CW)						
C/I_{Block}	Interfering signal frequency 30 MHz – 2000 MHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 10 MHz	-	5	-	dB
C/I_{Block}	Interfering signal frequency 2003 MHz – 2399 MHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 3 MHz	-	-5	-	dB
C/I_{Block}	Interfering signal frequency 2484 MHz – 2997 MHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 3 MHz	-	-5	-	dB
C/I_{Block}	Interfering signal frequency 3000 MHz – 12.75 GHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 25 MHz	-	10	-	dB
Intermodulation characteristics (CW signal at f_1, Bluetooth LE interfering signal at f_2)						
P_IM(3)	Input power of IM interferer at 3 and 6 MHz distance from wanted signal	Wanted signal = -64 dBm, PER < 30.8%	-	-27	-	dBm
P_IM(-3)	Input power of IM interferer at -3 and -6 MHz distance from wanted signal	Wanted signal = -64 dBm, PER < 30.8%	-	-40	-	dBm
P_IM(4)	Input power of IM interferer at ±4 and ±8 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%	-	-32	-	dBm
P_IM(5)	Input power of IM interferer at ±5 and ±10 MHz distance from wanted signal	Wanted signal = -64 dBm, PER < 30.8%	-	-32	-	dBm

Table 21. Bluetooth Low Energy RF receiver characteristics at 2 Msym/s uncoded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-94	-	dBm
P_{SAT}	Saturation	PER < 30.8%	-	8	-	dBm
Z_{RF1}	Optimum RF source (impedance at RF1 pin)	@ 2440 MHz	-	40	-	Ω
RF selectivity with Bluetooth LE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal= -67 dBm, PER < 30.8%	-	8	-	dBc
$C/I_{2\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -67 dBm, PER < 30.8%	-	-14	-	dBc
$C/I_{4\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 4$ MHz	Wanted signal = -67 dBm, PER < 30.8%	-	-41	-	dBc
$C/I_{6\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (6+2n)$ MHz [n = 0,1,2…]	Wanted signal = -67 dBm, PER < 30.8%	-	-45	-	dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image\text{-}2M}$	Wanted signal = -67 dBm, PER < 30.8%	-	-25	-	dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel-to-image frequency $f_{interference} = f_{image\text{-}2M} \pm 2$ MHz	Wanted signal= -67 dBm, PER < 30.8%	- / -	-14	-	dBc
Out of band blocking (interfering signal CW)						
C/I_{Block}	Interfering signal frequency 30 MHz – 2000 MHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 10 MHz	-	5	-	dB
C/I_{Block}	Interfering signal frequency 2003 MHz – 2399 MHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 3 MHz	-	-5	-	dB
C/I_{Block}	Interfering signal frequency 2484 MHz – 2997 MHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 3 MHz	-	-5	-	dB
C/I_{Block}	Interfering signal frequency 3000 MHz – 12.75 GHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 25 MHz	-	10	-	dB
Intermodulation characteristics (CW signal at f_1, Bluetooth LE interfering signal at f_2)						
P_IM(6)	Input power of IM interferer at 6 and 12 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%	-	-27	-	dBm
P_IM(-6)	Input power of IM interferer at -6 and -12 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%	-	-30	-	dBm
P_IM(8)	Input power of IM interferer at ±8 and ±16 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%	-	-30	-	dBm
P_IM(10)	Input power of IM interferer at ±10 and ±20 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%	-	-28	-	dBm

Table 22. **Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded (S=2)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-100	-	dBm
P_{SAT}	Saturation	PER < 30.8%		8	-	dBm
Z_{RF1}	Optimum RF source (impedance at RF1 pin)	@ 2440 MHz		40	-	Ω
RF selectivity with Bluetooth LE equal modulation on interfering signal						
C/I_{CO}-channel	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal = -72 dBm, PER < 30.8%	-	2	-	dBc
$C/I_{1\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz	Wanted signal = -72 dBm, PER < 30.8%		-5	-	dBc
$C/I_{2\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -72 dBm, PER < 30.8%		-38	-	dBc
$C/I_{3\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal = -72 dBm, PER < 30.8%		-50	-	dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image}$	Wanted signal = -72 dBm, PER < 30.8%		-30	-	dBc
$C/I_{Image\pm1}$ MHz	Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal = -72 dBm, PER < 30.8%		-34	-	dBc

Table 23. **Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded (S=8)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-104	-	dBm
P_{SAT}	Saturation	PER < 30.8%		8	-	dBm
Z_{RF1}	Optimum RF source (impedance at RF1 pin)	@ 2440 MHz		40	-	Ω
RF selectivity with Bluetooth LE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal = -72 dBm, PER < 30.8%	-	1	-	dBc
$C/I_{1\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz	Wanted signal = -72 dBm, PER < 30.8%		-4	-	dBc
$C/I_{2\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -72 dBm, PER < 30.8%		-39	-	dBc
$C/I_{3\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal = -72 dBm, PER < 30.8%		-53	-	dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image}$	Wanted signal = -72 dBm, PER < 30.8%		-33	-	dBc
$C/I_{Image} \pm 1$ MHz	Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal = -72 dBm, PER < 30.8%		-32	-	dBc

6.3.6 Embedded reset and power control block characteristics

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{RSTTEMPO}$	Reset temporization after PDR is detected	V_{DD} rising	-	-	500	µs
V_{PDR}	Power-down reset threshold	-	-	1.58	-	V
V_{PVD0}	PVD0 threshold	PVD0 threshold at the falling edge of V_{DDIO}	-	2.05	-	
V_{PVD1}	PVD1 threshold	PVD1 threshold at the falling edge of V_{DDIO}	-	2.21	-	
V_{PVD2}	PVD2 threshold	PVD2 threshold at the falling edge of V_{DDIO}	-	2.36	-	
V_{PVD3}	PVD3 threshold	PVD3 threshold at the falling edge of V_{DDIO}	-	2.53	-	
V_{PVD4}	PVD4 threshold	PVD4 threshold at the falling edge of V_{DDIO}	-	2.64	-	
V_{PVD5}	PVD5 threshold	PVD5 threshold at the falling edge of V_{DDIO}	-	2.82	-	
V_{PVD6}	PVD6 threshold	PVD6 threshold at the falling edge of V_{DDIO}	-	2.91	-	
V_{PVD7}	PVD threshold for V_{IN_PVD}	PVD7 threshold (VBGP) at the falling edge of V_{IN_PVD}	-	1	-	

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as: the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is put under the following conditions:

- all I/O pins are in analog input mode
- all peripherals are disabled except when explicitly mentioned
- the flash memory access time is adjusted with the minimum wait states number
- when the peripherals are enabled $f_{PCLK} = f_{HCLK}$

Table 25. Current consumption

Symbol	Parameter	Conditions	Typ.			Unit
			25 °C	85 °C	105 °C	
$I_{DD(Run)}$	Supply current in Run mode(1)	f_{HCLK} = 64 MHz All peripherals disabled	2474	2533	2580	µA
		f_{HCLK} = 32 MHz All peripherals disabled	1919	1980	2029	
		f_{HCLK} = 16 MHz All peripherals disabled	1576	1632	1678	
$I_{DD(Deepstop)}$	Supply current in Deepstop(2)	Clock OFF	654	3930	8870	nA
		Clock source LSI	1214	4556	9530	
		Clock source LSE	991	4828	10596	
I_{DD}(Shutdown)	Supply current in Shutdown	-	15	350	1090	
I_{DD}(RST)	Current under reset condition	-	1098	1160	1230	µA

1. *CPU executes a "while(1)" loop*
2. *The current consumption in Deepstop mode is measured considering the entire SRAM retained.*

6.3.8 Wake up time from low power modes

The wake up times reported are the latency between the event and the execution of the instruction. The device goes to low-power mode after WFI (wait for interrupt) instructions.

Table 26. Low power mode wake up timing

Symbol	Parameter	Conditions	Typ.	Unit
$T_{WUDEEPSTOP}$	Wake up time from Deepstop mode to Run mode	Wake up from GPIO V_{DD} = 3.3 V flash memory	170	µs

6.3.9 High speed crystal requirements

The high speed external oscillator must be supplied with an external 32 MHz crystal that is specified for a 6 to 8 pF loading capacitor. The STM32WB05xN includes internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one. These internal load capacitors are made by a fixed one, in parallel with a 6-bit binary weighted capacitor bank. Thanks to low CL step size (1-bit is typically 0.07 pF), very fine crystal tuning is possible. With a typical crystal sensitivity of -14 ppm/pF, it is possible to trim a 32 MHz crystal, with a resolution of 1 ppm.

The requirements for the external 32 MHz crystal are reported in the table below.

Table 27. HSE crystal requirements

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Oscillator frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance	-	-	±50	ppm
ESR	Equivalent series resistance	-	-	-	100	Ω
P_D	Drive level	-	-	-	100	µW
CL	HSE crystal load capacitance	27 °C, typical corner GMCONF = 3	5 [1]	7[2]	9.2[3]	pF
CLstep	HSE crystal load capacitance 1-bit value	27 °C, GMCONF = 3 XOTUNE code between 32 and 33	-	0.07	-	pF

1. *XOTUNE programed at minimum code = 0*
2. *XOTUNE programed at center code = 32*
3. *XOTUNE programed at maximum code = 63*

6.3.10 Low speed crystal requirements

Low speed clock can be supplied with an external 32.768 kHz crystal oscillator. Requirements for the external 32.768 kHz crystal are reported in the table below.

Table 28. LSE crystal requirements

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency	-	-	32.768	-	kHz
ESR	Equivalent series resistance	-	-	-	90	kΩ
P_D	Drive level	-	-	-	0.1	µW
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 00 Low drive capability	-	-	0.50	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.70	µA/V
		LSEDRV[1:0] = 11 High drive capability	-	-	2.70	

6.3.11 High speed ring oscillator characteristics

Table 29. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency	-	-	64	-	MHz

6.3.12 Low speed ring oscillator characteristics

Table 30. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency	-	-	33	-	kHz
$\Delta F_{RO\_\Delta T}/F_{RO}$	Frequency spread vs. temperature	Standard deviation	-	140	-	ppm/°C

6.3.13 PLL characteristics

Characteristics measured over recommended operating conditions unless otherwise specified.

Table 31. PLL characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PN_{SYNTH}	RF carrier phase noise	At ±1 MHz offset from carrier (measured at 2.4 GHz)	-	-110	-	dBc/Hz
		At 2.4 GHz ±3 MHz offset from carrier (measured at 2.4 GHz)	-	-114	-	dBc/Hz
		At 2.4 GHz±6 MHz offset from carrier (measured at 2.4 GHz)	-	-128	-	dBc/Hz
		At ±25 MHz offset from carrier	-	-135	-	dBc/Hz
$LOCK_{TIMETX}$	PLL lock time to TX	With calibration @2.5 ppm	-	150	-	µs
$LOCK_{TIMERX}$	PLL lock time to RX	With calibration @2.5 ppm	-	110	-	µs
$LOCK_{TIMERXTX}$	PLL lock time RX to TX	Without calibration @2.5 ppm	-	47	-	µs
$LOCK_{TIMETXRX}$	PLL lock time TX to RX	Without calibration @2.5 ppm	-	32	-	µs

6.3.14 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n + 1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 32. **ESD absolute maximum ratings**

Symbol	Parameter	Conditions	Class	Max.(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	Conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CBM)}$	Electrostatic discharge voltage (charge device model)	Conforming to ANSI/ESDA/STM5.3.1 JS-002	C2a	500	

1. *Guaranteed by design.*

6.3.15 I/O port characteristics

Unless otherwise specified, the parameters given in the tables below are derived from tests performed under the conditions summarized in Table 15. General operating conditions. All I/Os are designed as CMOS-compliant.

Table 33. **I/O static characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	1.62 V < V_{DD} < 3.6 V	-	-	0.3 x V_{DD}	V
V_{IH}	I/O input high level voltage		0.7 x V_{DD}	-	-	
I_{lkg}	Input leakage current	0 <= V_{IN} <= Max(V_{DDx})(1)	-	-	+/-100	nA
		Max(V_{DDx})(1) <= V_{IN} <= Max(V_{DDx})(1) +1 V	-	-	650	
		Max(V_{DDx})(1) + 1 V < V_{IN} <= 5.5 V	-	-	200	
R_{PU}	Pull-up resistor	V_{IN} = GND	25	40	55	kΩ
R_{PD}	Pull-down resistor	V_{IN} = VDD	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Max(V_{DDx}) is the maximum value among all the I/O supplies.*

All I/Os are CMOS-compliant (no software configuration required).

GPIOs (general purpose input/outputs) can sink or source up to ±8 mA and sink or source up to ± 20 mA (with a relaxed V_{OL} / V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified.

- The sum of currents sourced by all I/Os on VDD, plus the maximum consumption of MCU sourced on VDD, cannot exceed the absolute maximum rating ΣIVDD
- The sum of currents sunk by all I/Os on VSS, plus the maximum consumption of the MCU sunk on GND, cannot exceed the absolute maximum rating ΣIVGND.

Table 34. **Output voltage characteristics**

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}	Output low level voltage for I/O pin	CMOS port(1) |IIO| = 8 mA VDD ≥ 2.7 V	-	0.4	V
V_{OH}	Output high level voltage for I/O pin		VDD -0.4	-	
V_{OL}	Output low level voltage for I/O pin	|IIO| = 20 mA VDD ≥ 2.7 V	-	1.3	
V_{OH}	Output high level voltage for I/O pin		VDD -1.3	-	
V_{OL}	Output low level voltage for I/O pin	|IIO| = 4 mA VDD ≥ 1.62 V	-	0.4	
V_{OH}	Output high level voltage for I/O pin		VDD-0.45	-	

1. *CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*

6.3.16 RSTN pin characteristics

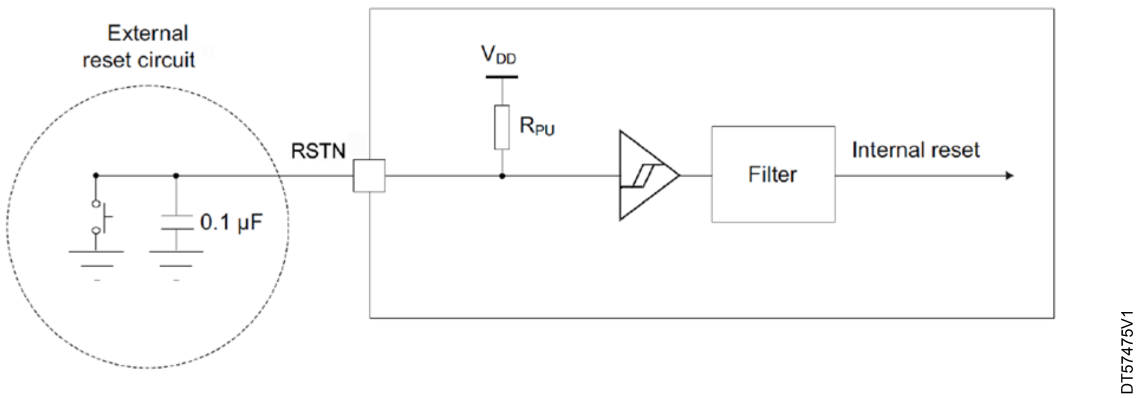
The RSTN pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 6.3.2: General operating conditions.

Table 35. RSTN pin characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
$V_{IL(RSTN)}$	RSTN input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(RSTN)}$	RSTN input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(RSTN)}$	RSTN Schmitt trigger voltage hysteresis	-	-	200	-	mV
RPU	Weak pull-up equivalent resistor	V_{IN}=GND	25	40	55	kΩ

Figure 9. Recommended RSTN pin protection



Note: The external reset circuit protects the device against parasitic resets.
The user must ensure that the level on the RSTN pin can go below the V_{IL}(RSTN) max. level specified in the table, otherwise the reset is not taken into account by the device. The external capacitor on RSTN must be placed as close as possible to the device.

6.3.17 SPI characteristics

The parameters for SPI are derived from tests performed according to f_{PCLKx} frequency and supply voltage conditions summarized in Table 15. General operating conditions.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Table 36. SPI characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCK}	SPI clock frequency	Master mode	-	-	32	MHz
		Slave mode			32(1)	
tsu(NSS)	NSS setup time	-	4 / f_{PCLK}	-	-	-
th(NSS)	NSS hold time	-	2 / f_{PCLK}	-	-	-
tw(SCKH), tw(SCKL)	SCK high and low time	Master mode	1 / f_{PCLK} - 1.5	1 / f_{PCLK}	1 / f_{PCLK}+1	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tsu(MI)	Data input set-up time	Master mode	2	-	-	ns
tsu(SI)	Data input set-up time	Slave mode	1	-	-	
th(MI)	Data input hold time	Master mode	2	-	-	
th(SI)	Data input hold time	Slave mode	0	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	6	-	30	
$t_{dis(SO)}$	Data output disable time	Slave mode	6	-	32	
$t_{v(MO)}$	Data output valid time	Master mode	-	5	9	
$t_{v(SO)}$		Slave mode	-	12	35	
$t_{h(MO)}$	Data output hold time	Master mode	1	-	-	
$t_{h(SO)}$		Slave mode	6	-		

1. *The maximum frequency in slave transmitter mode is determined by the sum of tv(SO) and tsu(MI), which has to fit SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while duty(SCK) = 50 %.*

Figure 10. SPI timing diagram - slave mode and CPHA = 0

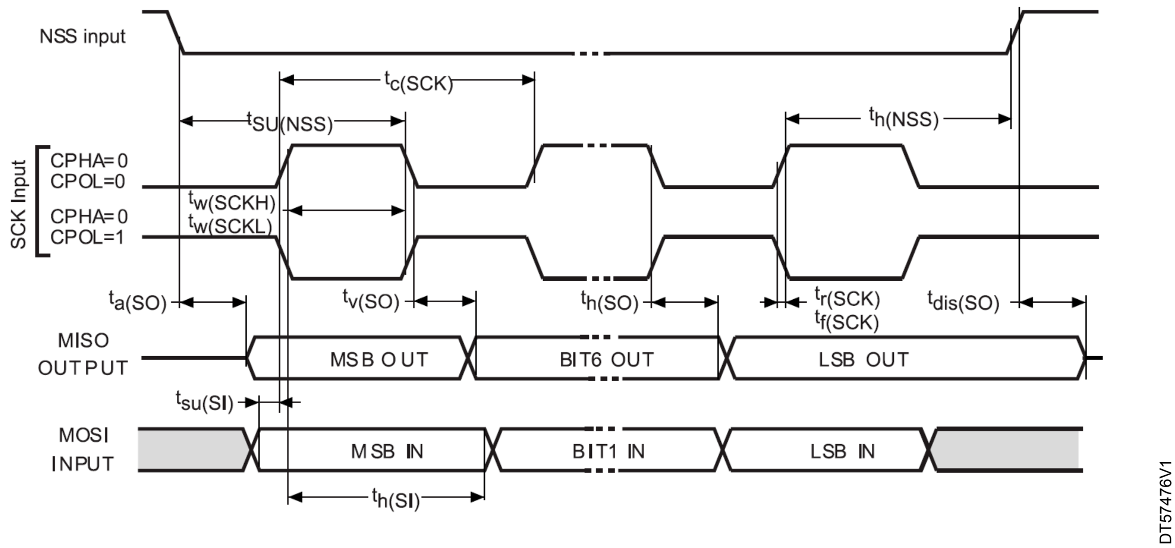


Figure 11. SPI timing diagram - slave mode and CPHA = 1

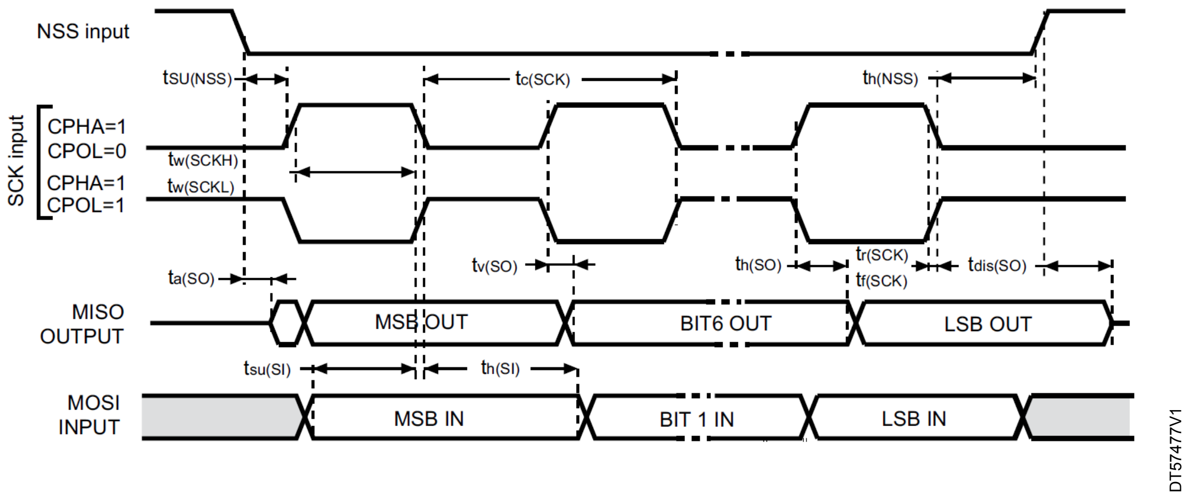
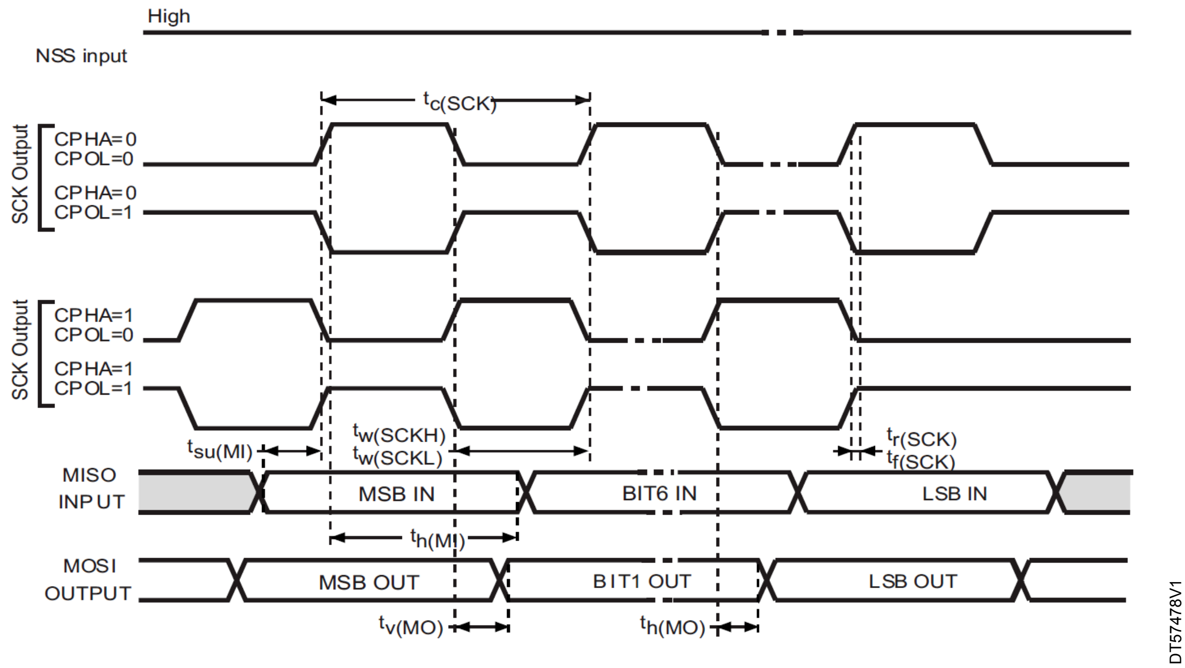


Figure 12. SPI timing diagram - master mode



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 Device marking

Refer to technical note *"Reference device marking schematics for STM32 microcontrollers and microprocessors"* (TN1433) available on http://www.st.com. This note provides information on the location of pin 1 / ball A1 and the location and orientation of the marking areas relative to pin 1 / ball A1.

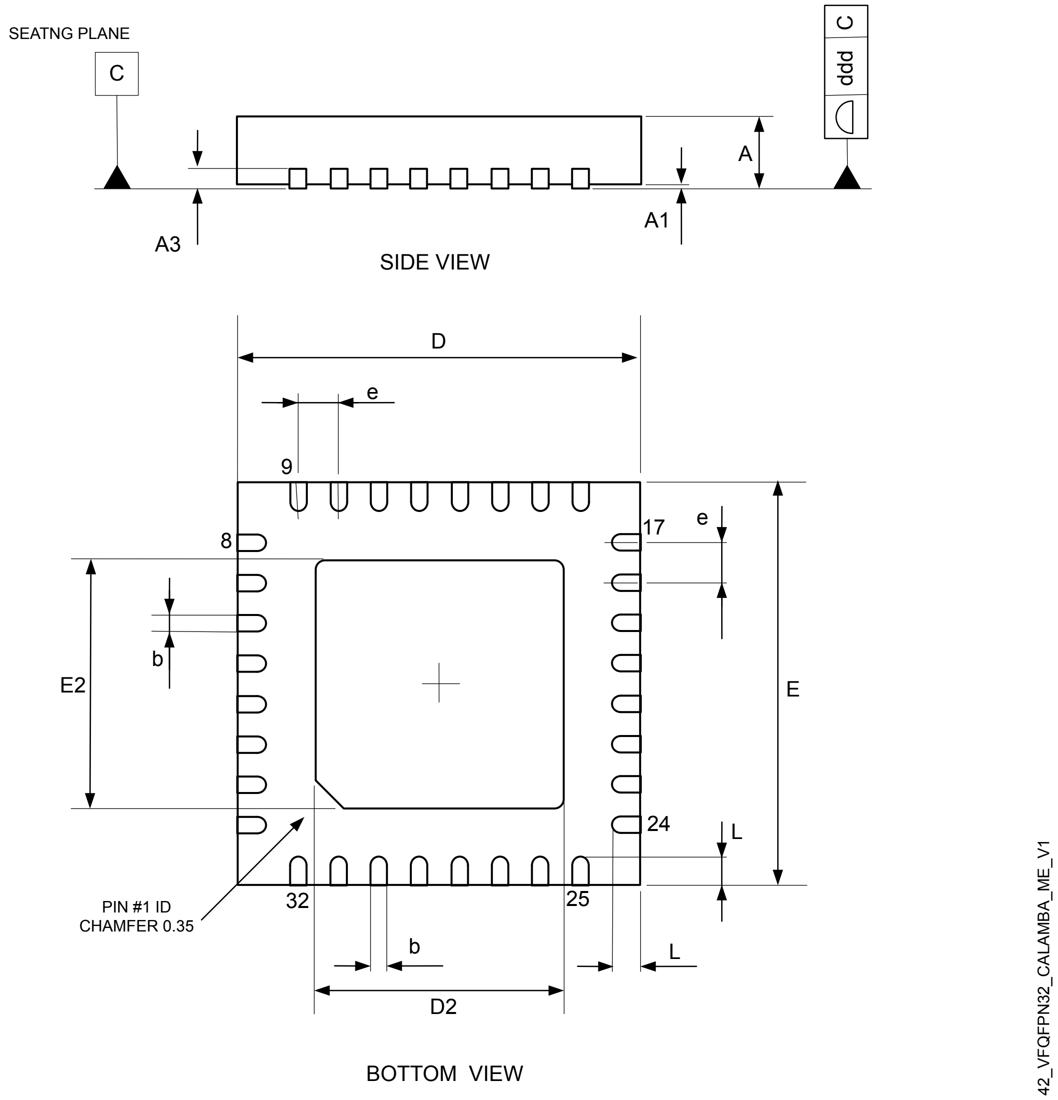
Parts marked as ES, E, or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event, STMicroelectronics is liable for the customer using any of these engineering samples in production. STMicroelectronics quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example is provided in the corresponding package information subsection.

7.2 VFQFPN32 package information (42)

This VFQFPN is a 32 lead, 5 x 5 mm, 0.50 mm pitch, very fine pitch quad flat no lead package.

Figure 13. VFQFPN32 - Outline



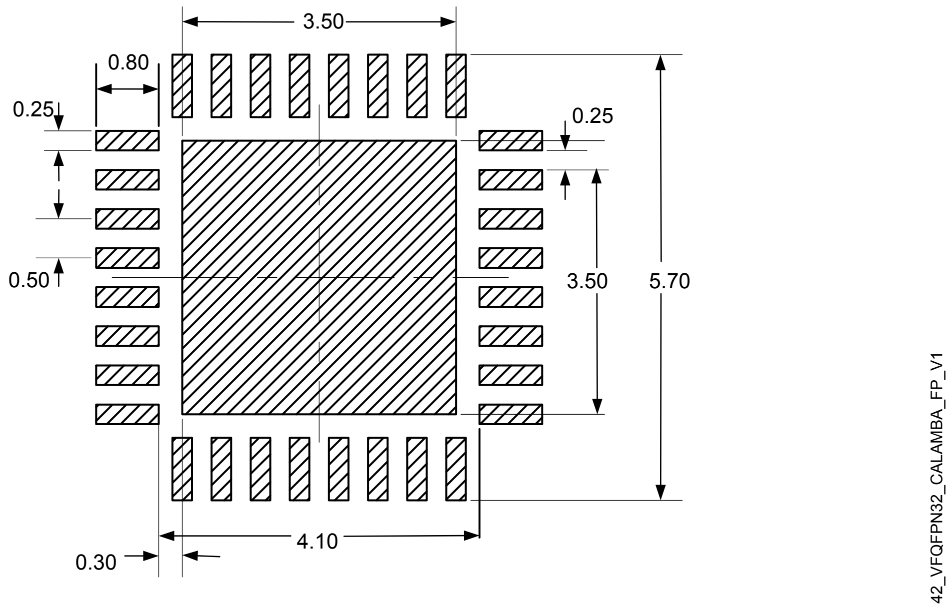
1. *Drawing is not to scale.*
2. *Package outline exclusive of any mold flashes dimensions and metal burrs.*
3. *Details of terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.*

Table 37. VFQFPN32 - Mechanical data

Symbol	Millimetres			Inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	-	0.05	0	-	0.0020
A3	-	0.20	-	-	0.008	-
b	0.18	0.25	0.30	0.0070	0.0098	0.0118
D	4.90	5.00	5.10	0.1929	0.19	0.2008
E	4.90	5.00	5.10	0.1929	0.19	0.2008
D2	3.60	3.70	3.80	0.1417	0.1457	0.1496
E2	3.60	3.70	3.80	0.1417	0.1457	0.1496
e	-	0.50	-	-	0.0197	-
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd	-	-	0.05	-	-	0.0020

1. *Values in inches are converted from mm and rounded to 3 decimal digits.*
2. *VFQFPN stands for thermally Enhanced very thin fine pitch quad flat package No lead . Very thin profile 0.80 < A ≤ 1.00 mm.*

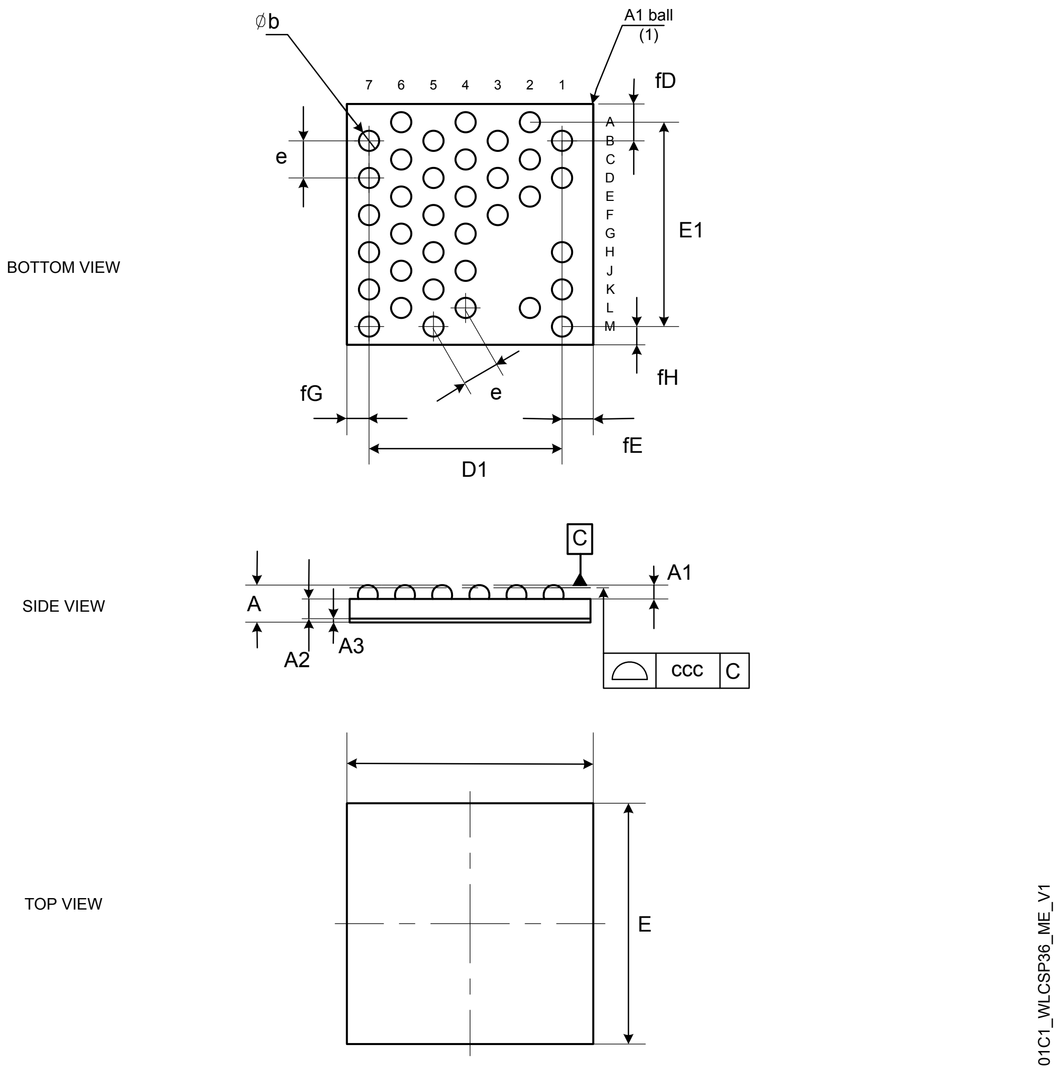
Figure 14. VFQFPN32 - Footprint example



7.3 WLCSP36 package information (01C1)

This WLCSP is a 36-ball, 2.652 x 2.592 mm, 0.40 mm pitch, wafer level chip scale array package.

Figure 15. **WLCSP36 - Outline**



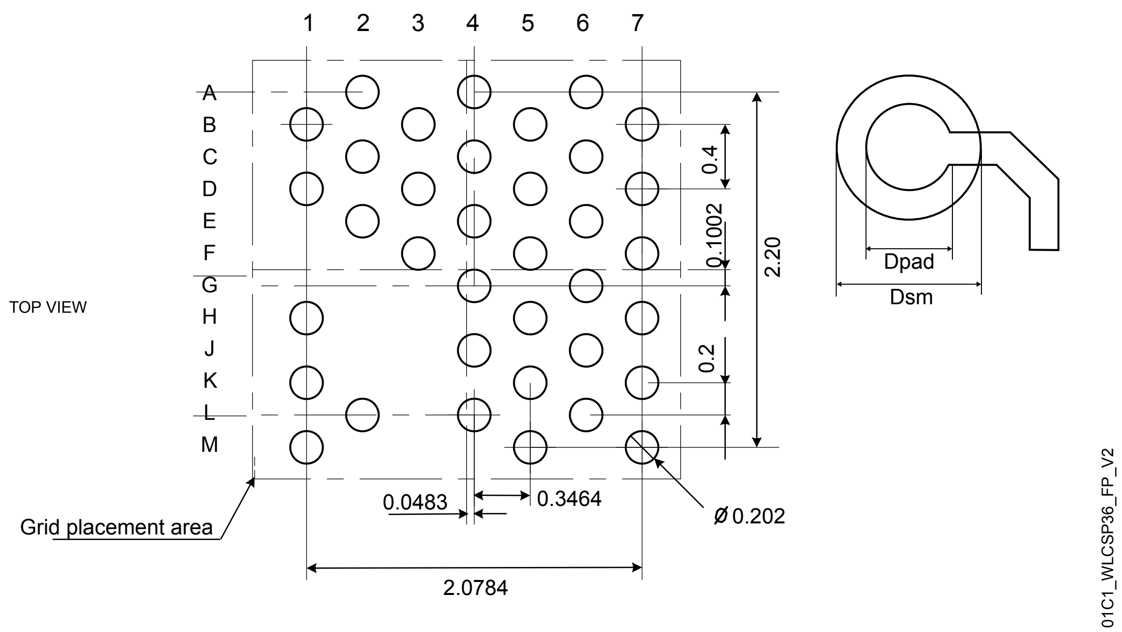
1. *The terminal A1 on the bumps side is identified by a distinguishing feature (for instance by a circular "clear area" - typically 0.1 mm diameter) and/or a missing bump.*
   The terminal A1 on the backside of the product is identified by a distinguishing feature (for instance by a circular "clear area" - typically 0.5 mm diameter).
2. *Drawing is not to scale.*

Table 38. WLCSP36 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.422	-	-	0.0166
A1	0.135	-	-	0.0053	-	-
A2	-	0.225	-	-	0.0088	-
A3	-	0.025	-	-	0.0010	-
b	0.193	0.218	0.243	0.0076	0.0085	0.0096
D	-	2.652	-	-	0.1044	-
D1	-	2.078	-	-	0.0818	-
E	-	2.592	-	-	0.1020	-
E1	-	2.200	-	-	0.0866	-
e	-	0.40	-	-	0.0157	-
fD	-	0.397	-	-	0.0156	-
fE	-	0.335	-	-	0.0132	-
fG	-	0.239	-	-	0.0094	-
fH	-	0.196	-	-	0.0077	-
ccc	-	0.030	-	-	0.0012	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 16. WLCSP36 - Footprint example



1. *Dimensions are expressed in millimeters.*

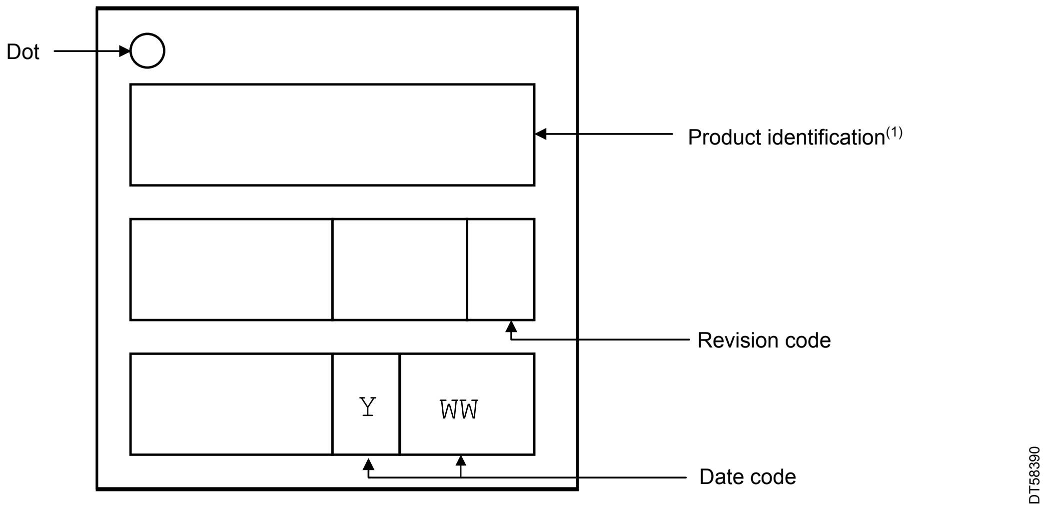
Table 39. WLCSP36 - Example of PCB design rules

Dimension	Values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

7.3.1 Device marking example for WLCSP36

The following figure gives an example of topside marking versus pin 1 position identifier location. The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 17. WLCSP36 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax.}$) must never exceed the values in general operating conditions.

The maximum chip-junction temperature, T_J max., in degrees Celsius, can be calculated using the equation:

$$T_J\text{max.} = T_A\text{max.} + (PD\text{max} \times \theta JA) \quad (1)$$

where:

- T_A max. is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W
- PD max. is the sum of PINT max. and PI/O max. (PD max. = PINT max. + PI/O max.)
- PINT max. is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power

PI/O max represents the maximum power dissipation on output pins:

- PI/O max. = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the applications.

Note: When the SMPS is used, a portion of the power consumption is dissipated into the external inductor, therefore reducing the chip power dissipation. This portion depends mainly on the inductor ESR characteristics.

Note: As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the chip power consumption.

Note: RF characteristics (such as: sensitivity, Tx power, consumption) are provided up to 85 °C.

Table 40. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient VFQFPN32 - 5 mm x 5 mm	26.9	°C/W
	Thermal resistance junction-ambient WLCSP36 - 0.4 mm pitch	-[1]	

1. *Not yet available.*

8 Ordering information

Table 41. Ordering information scheme

Example:	STM32	WB	05	K	N	V	6	TR
Device family								
STM32 = Arm-based 32-bit microcontroller								
Product type								
WB = wireless Bluetooth®								
Device subfamily								
05 = full set of features								
Pin count								
K = 32 pins								
T = 36 pins								
Network coprocessor								
N = network coprocessor								
Package(1)								
F = WLCSP ECOPACK2								
V = VFQFPN ECOPACK2								
Temperature range								
6 = -40 °C up to +85 °C								
7 = -40 °C up to +105 °C								
Packing								
TR = tape and reel								

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*

Note: For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 42. **Document revision history**

Date	Version	Changes
17-Jun-2024	1	Initial release.
26-Jun-2024	2	Updated various sections.

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