12-Bit 16-Channel 1-MSPS SAR ADC

Features

- AEC-Q100 Qualified for Automotive Applications:
  - Grade 1: −40°C to 125°C T_A
- 16-Channel 12-Bit SAR ADC
  - 0 to 2.5 V and 0 to 5 V range
  - Programmable Out-of-Range Alarms
  - 1-MHz Sample Rate Serial Devices
- General Purpose I/O Ports (GPIOs)
- Low-Power SPI-Compatible Serial Interface
- Compact TSSOP-38 Package
- Operating Temperature: –40°C to 125°C

Applications

- Automotive
- Status Monitoring
- Data Acquisition Systems

Description

The TPC5120Q includes a capacitor-based SAR A/D converter with inherent sample and hold. TPC5120Q has 16 channel single-ended inputs.

The devices accept a wide analog supply range from 2.7 V to 5.25 V. Very low power consumption makes these devices suitable for battery-powered and isolated power-supply applications.

A wide 1.7-V to 5.25-V I/O supply range facilitates a glueless interface with the most commonly used digital hosts. The serial interface is controlled by $\overline{CS}$ and SCLK to make it easy to connect with microprocessors and DSP.

The input signal is sampled with the falling edge of $\overline{CS}$. It uses SCLK for conversion, serial data output, and reading serial data in. The devices allow auto sequencing of preselected channels or manual selection of a channel for the next conversion cycle. There are two software-selectable input ranges (0 V to V_{REF} and 0 V to 2 x V_{REF}), individually configurable GPIOs, and two programmable alarm thresholds per channel. These features make the devices suitable for most data acquisition applications.

The devices offer an attractive power-down feature. This is extremely useful for power saving when the device is operated at lower conversion speeds.

Functional Block Diagram

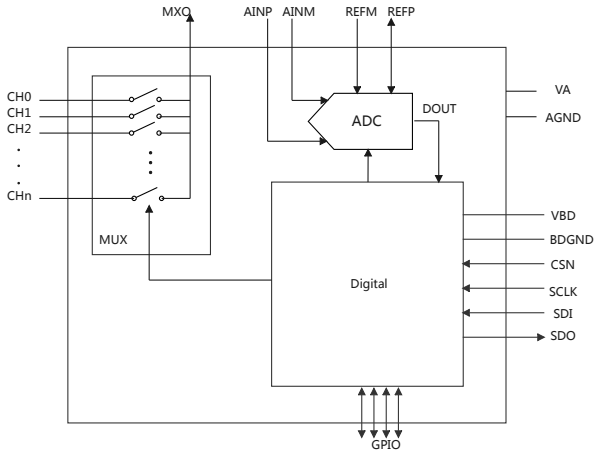


Figure 1. TPC5120Q Block Diagram

Table of Contents

Features **1**
Applications **1**
Description **1**
Functional Block Diagram **1**
Product Family Table **3**
Revision History **3**
Pin Configuration and Functions **4**
Specifications **6**
Absolute Maximum Ratings (1) 6
ESD, Electrostatic Discharge Protection 6
Recommended Operating Conditions 6
Thermal Information 6
Electrical Characteristics 7
Timing Requirements 9
Typical Performance Characteristics 11
Detailed Description **12**
Overview 12
Functional Block Diagram 13
Feature Description 14
Programming 18
Application and Implementation **27**
Application Information 27
Tape and Reel Information **29**
Package Outline Dimensions **30**
TSSOP-38 30
Order Information **31**
IMPORTANT NOTICE AND DISCLAIMER **32**

Product Family Table

Order Number	Channels	Resolution	Throughput	Package
TPC5120Q-TS7R-S	16	12 bits	1 MSPS	TSSOP-38

Revision History

Date	Revision	Notes
2023-12-26	Rev.A.0	Initial release.

Pin Configuration and Functions

TPC5120Q
TSSOP-38 Package
Top View

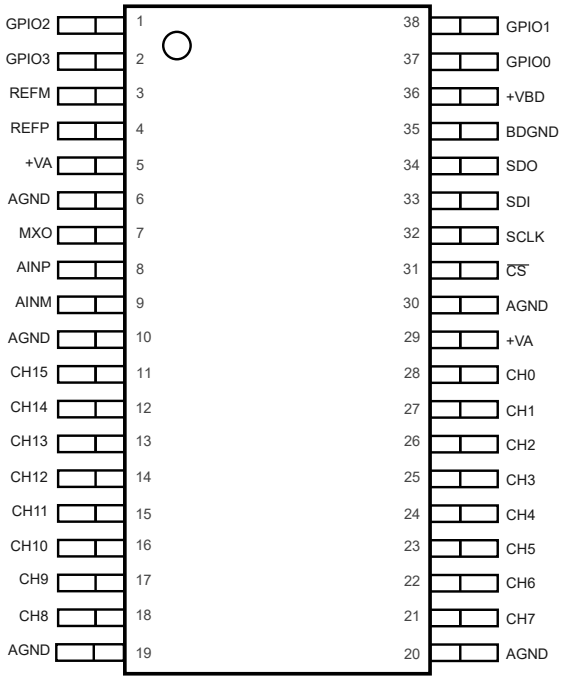


Table 1. Pin Functions: TPC5120Q

TPC5120Q		I/O	Description
Pin Number	Pin Name		
3	REFM	Analog input	Reference ground
4	REFP	Analog input	Reference input
8	AINP	Analog input	ADC input signal
9	AINM	Analog input	ADC input ground
7	MXO	Analog output	Multiplexer output
28	Ch0	Analog input	Analog channel for multiplexer
27	Ch1	Analog input	Analog channel for multiplexer
26	Ch2	Analog input	Analog channel for multiplexer
25	Ch3	Analog input	Analog channel for multiplexer
24	Ch4	Analog input	Analog channel for multiplexer
23	Ch5	Analog input	Analog channel for multiplexer
22	Ch6	Analog input	Analog channel for multiplexer
21	Ch7	Analog input	Analog channel for multiplexer
18	Ch8	Analog input	Analog channel for multiplexer
17	Ch9	Analog input	Analog channel for multiplexer

TPC5120Q		I/O	Description
Pin Number	Pin Name		
16	Ch10	Analog input	Analog channel for multiplexer
15	Ch11	Analog input	Analog channel for multiplexer
14	Ch12	Analog input	Analog channel for multiplexer
13	Ch13	Analog input	Analog channel for multiplexer
12	Ch14	Analog input	Analog channel for multiplexer
11	Ch15	Analog input	Analog channel for multiplexer
31	$\overline{CS}$	Digital input	Chip-select input pin; active low
32	SCLK	Digital input	Serial clock input pin
33	SDI	Digital input	Serial data input pin
34	SDO	Digital output	Serial data output pin
37	GPIO0	Digital I/O	General-purpose input or output
	Alarm	Digital output	Active high alarm output.
38	GPIO1	Digital I/O	General-purpose input or output
	Low alarm	Digital output	Active high output indicating low alarm
1	GPIO2	Digital I/O	General-purpose input or output
	Range	Digital input	Select ADC input range: High → Range 2 (0 to 2 x V_{REF}) Low → Range 1 (0 to V_{REF})
2	GPIO3	Digital I/O	General-purpose input or output
	PD	Digital input	Active low power-down input
5, 29	$+V_A$	—	Analog power supply
6, 10, 19, 20, 30	AGND	—	Analog ground
36	$+V_{BD}$	—	Digital I/O supply
35	BDGND	—	Digital ground

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Analog Voltage	AINP or CHn to AGND	–0.3	V_A +0.3	V
Digital Voltage	Digital input voltage to BDGND	–0.3	7	V
	Digital output to BDGND	–0.3	V_A + 0.3	V
Supply Voltage	+V_A to AGND, +V_{BD} to BDGND	–0.3	7	V
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_A	Analog power-supply voltage	2.7		5.25	V
V_{BD}	Digital I/O-supply voltage	1.7	3.3	V_{VA}	V
V_{REF}	Reference voltage	2	2.5	V_A	V
f_{SCLK}	SCLK frequency		20		MHz
T_A	Operating temperature range	−40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
TSSOP-38	83.6	29.8	44.7	°C/W

Electrical Characteristics

All test condition is $+V_A$ = 2.7 V to 5.25 V, $+V_{BD}$ = 1.7 V to V_A, V_{REF} = 2.5 V ± 0.1V, T_A = –40℃ to 125℃, f_{sample} = 1 MHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
ANALOG INPUT					
Full-scale input span	Range 1	0		V_{REF}	V
	Range 2 while $2V_{REF} \le +V_A$	0		$2*V_{REF}$	V
Absolute input range (1)	Range 1	−0.2		V_{REF}+0.2	V
	Range 2 while $2V_{REF} \le +V_A$	−0.2		$2*V_{REF}$+0.2	V
Input capacitance			22		pF
Input leakage current	T_A = 25 ℃		30		nA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Code Resolution		12			Bits
Integral linearity	Fsample = 1 MHz	−1.5		1.5	LSB
Differential linearity	Fsample = 1 MHz	−0.99		1.5	LSB
Offset error		−5	±0.5	5	LSB
Total unadjusted error (TUE)			±3		LSB
Gain error		–4	±1	4	LSB
SAMPLING DYNAMICS					
Conversion time	20 MHz sclk			800	ns
Acquisition time		300			ns
Maximum throughput rate	20 MHz sclk			1	MHz
Aperture delay			5		ns
DYNAMIC CHARACTERISTICS					
Total harmonic distortion	100 kHz, –1dB input		−82		dB
Signal-to-noise ratio	100 kHz, –1dB input		71		dB
Signal-to-noise + distortion	100 kHz, –1dB input		70		dB
Small signal bandwidth	100 kHz, –1dB input		47		MHz
Channel-to-channel crosstalk	All off-channel with 100 kHz, Full-scale input to channel being sampled with DC input (isolation crosstalk).		−80		dB
	From previously sampled to channel with 100 kHz, Full-scale input to channel being sampled with DC input (memory crosstalk).		–80		dB
EXTERNAL REFERENCE INPUT					

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{REF} reference voltage at REFP		2	2.5	V_A	V
Reference resistance	Fsample = 1 MHz		16		kΩ
ALARM SETTING					
Higher threshold range		0		FFC	Hex
Lower threshold range		0		FFC	Hex
DIGITAL INPUT/OUTPUT					
Logic family	CMOS				
V_{IH}		0.7*(+V_{BD})			V
V_{IL}	+V_{BD} = 5 V			0.3*V_{BD}	V
V_{OH}	At I_{source} = 200 μA	V_{BD}-0.2			V
V_{OL}	At I_{sink} = 200 μA			0.4	V
Data format MSB first		MSB first			
POWER SUPPLY REQUIREMENTS					
+V_A supply voltage		2.7	3.3	5.25	V
+V_{BD} supply voltage		1.7	3.3	5.25	V
Supply current (Normal mode)	1 MSPS throughput		3.8		mA
	static state		1.65		mA
Power-down state supply current			10		μA
+V_{BD} supply current	+V_A = 5.25 V, f_s = 1 MHz		1		mA
Power-up time			1		μs
Invalid conversions after power up or reset			1		Numbers
TEMPERATURE RANGE					
Temperature Range	Specified performance	−40		+125	℃

(1) Parameters are provided by design simulation.

Timing Requirements

All parameters are provided by design simulation, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
t_{conv}	Conversion time	$+V_{BD}$= 1.8 V			16	SCLK
		+ V_{BD}= 3 V			16	
		+ V_{BD}= 5 V			16	
t_q	Minimum quiet sampling time needed from bus 3-state to start of next conversion	+ V_{BD}= 1.8 V	40			ns
		+ V_{BD}= 3 V	40			
		+ V_{BD}= 5 V	40			
t_{d1}	Delay time, $\overline{CS}$ low to first data (DO–15) out	+ V_{BD}= 1.8 V			38	ns
		+ V_{BD}= 3 V			27	
		+ V_{BD}= 5 V			17	
t_{su1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	+ V_{BD}= 1.8 V	8			ns
		+ V_{BD}= 3 V	6			
		+ V_{BD}= 5 V	4			
t_{d2}	Delay time, SCLK falling to SDO next data bit valid	+ V_{BD}= 1.8 V			35	ns
		+ V_{BD}= 3 V			27	
		+ V_{BD}= 5 V			17	
t_{h1}	Hold time, SCLK falling to SDO data bit valid	+ V_{BD}= 1.8 V	7			ns
		+ V_{BD}= 3 V	5			
		+ V_{BD}= 5 V	3			
t_{d3}	Delay time, 16^{th} SCLK falling edge to SDO 3-state	+ V_{BD}= 1.8 V			26	ns
		+ V_{BD}= 3 V			22	
		+ V_{BD}= 5 V			13	
t_{su2}	Setup time, SDI valid to rising edge of SCLK	+ V_{BD}= 1.8 V	2			ns
		+ V_{BD}= 3 V	3			
		+ V_{BD}= 5 V	4			
t_{h2}	Hold time, rising edge of SCLK to SDI valid	+ V_{BD}= 1.8 V	12			ns
		+ V_{BD}= 3 V	10			
		+ V_{BD}= 5 V	6			
t_{w1}	Pulse duration $\overline{CS}$ high	+ V_{BD}= 1.8 V	20			ns
		+ V_{BD}= 3 V	20			
		+ V_{BD}= 5 V	20			
t_{d4}	Delay time $\overline{CS}$ high to SDO 3-state	+ V_{BD}= 1.8 V			24	ns
		+ V_{BD}= 3 V			21	
		+ V_{BD}= 5 V			12	
t_{wh}	Pulse duration SCLK high	+ V_{BD}= 1.8 V	20			ns

Parameter		Conditions	Min	Typ	Max	Unit
		+ V_{BD}= 3 V	20			
		+ V_{BD}= 5 V	20			
t_{wl}	Pulse duration SCLK low	+ V_{BD}= 1.8 V	20			ns
		+ V_{BD}= 3 V	20			
		+ V_{BD}= 5 V	20			
Frequency SCLK		+ V_{BD}= 1.8 V			20	MHz
		+ V_{BD}= 3 V			20	
		+ V_{BD}= 5 V			20	

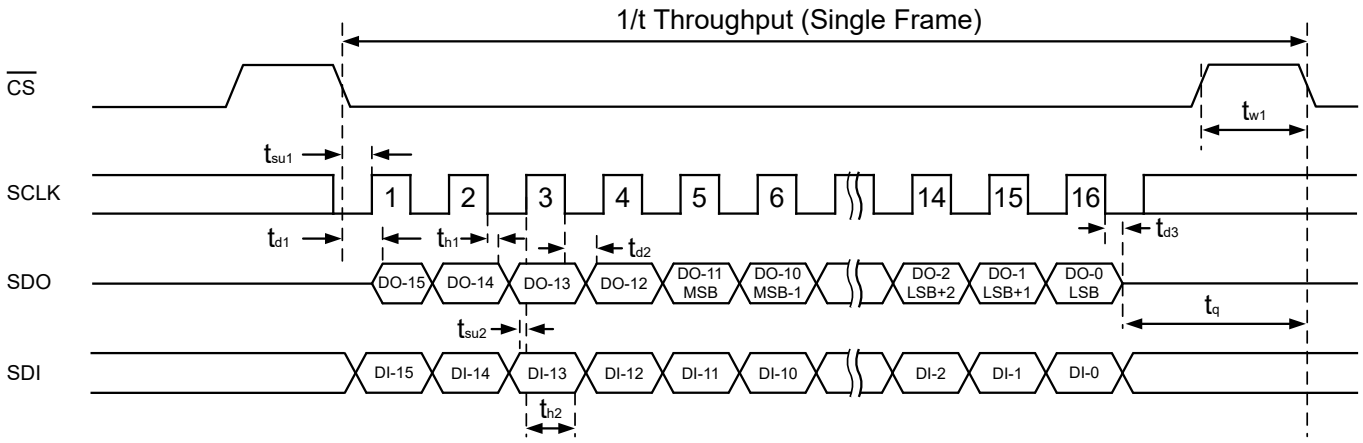


Figure 2. Serial Interface Timing Diagram

Typical Performance Characteristics

All test condition is $+V_A$ = 5 V, $+V_{BD}$ = 5 V, T_A = +25°C, unless otherwise noted.

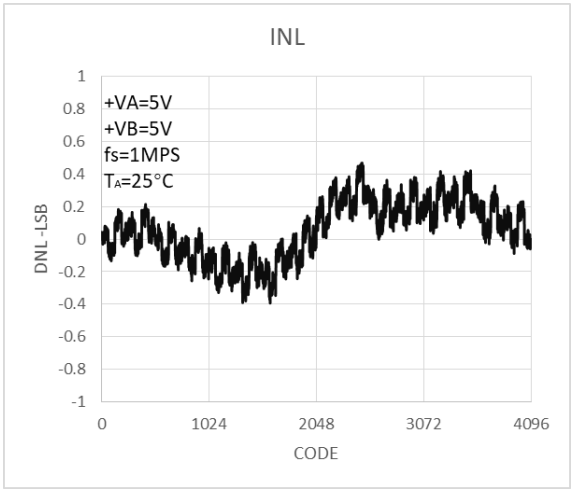


Figure 3. INL

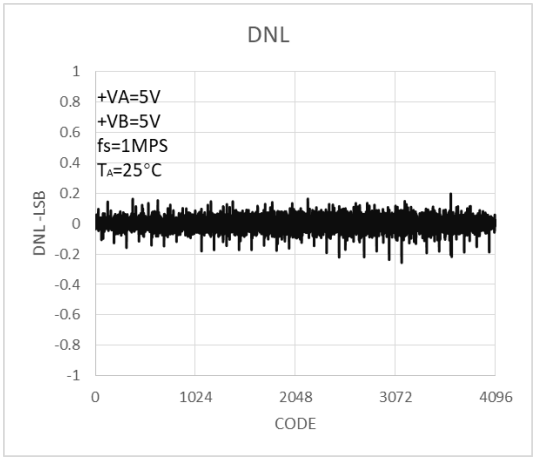


Figure 4. DNL

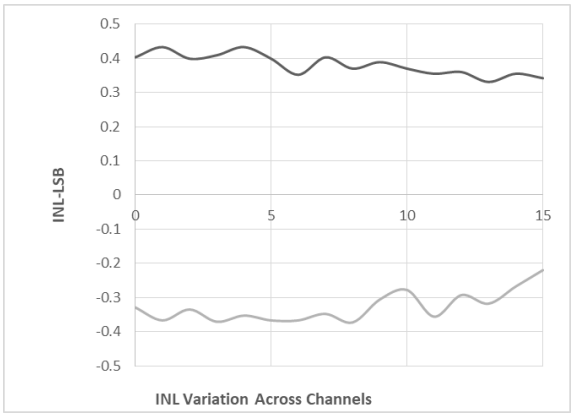


Figure 5. INL across Channels

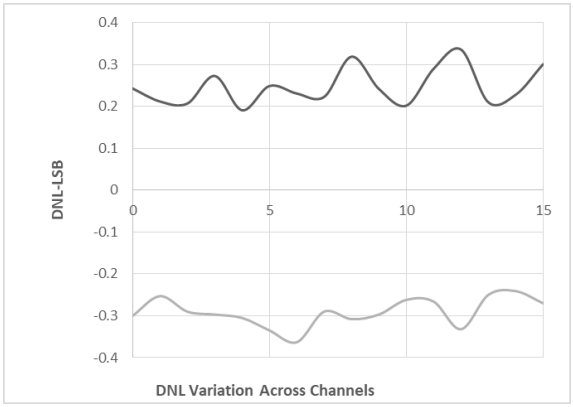


Figure 6. DNL across Channels

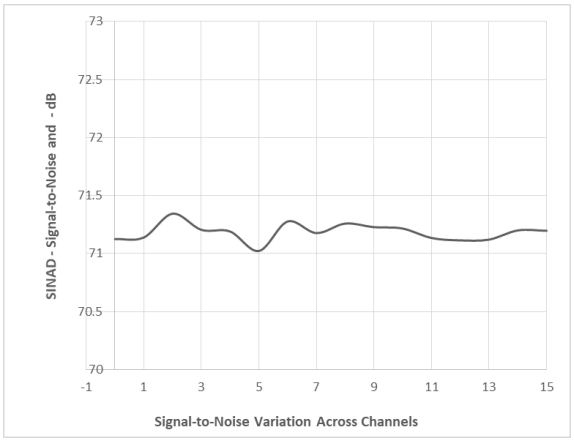


Figure 7. SNR across Channels

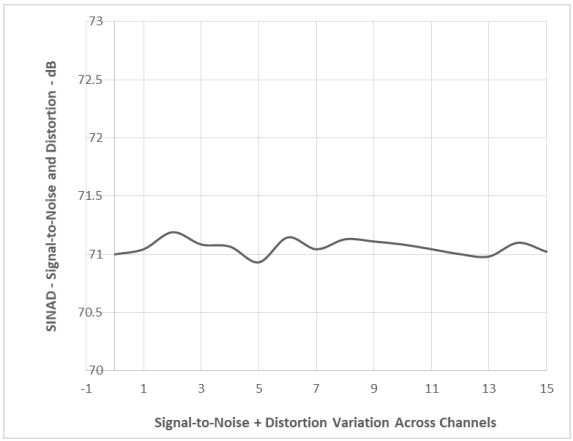


Figure 8. SINAD across Channels

Detailed Description

Overview

The TPC5120Q is a 12-bit multichannel, high-speed, low-power, real-time-converting, capacitor-based, and successive approximation register (SAR) analog-to-digital converter (ADC) that uses external references.

The architecture is based on capacitor charge redistribution, which inherently includes a sample/hold function. The sampling point can be controlled with great precision in time by CSN's falling edge.

The analog inputs to the TPC5120Q are provided to CHx input channels, all input channels share a common reference ground (AINM). The TPC5120Q has a multiplexer breakout feature which allows to connect with the signal conditioning circuit between the multiplexer output (MXO) and the ADC input (AINP). This feature enables the use of a common signal conditioning block for the input signal which exhibits similar performance characteristics.

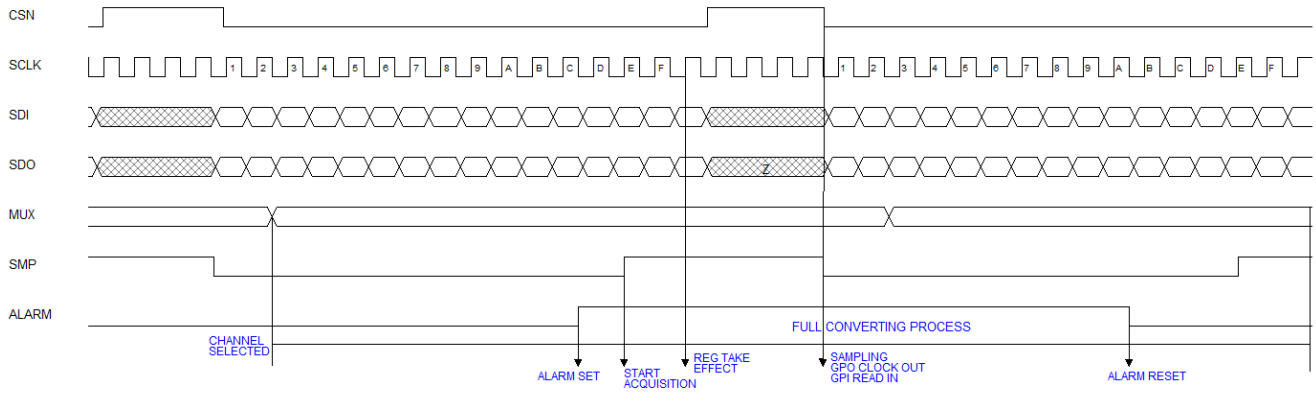


Figure 9. Operation Timing Diagram

The TPC5120Q can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep through the input channels automatically.

Each frame begins with the falling edge of CSN. With the falling edge of CSN, the input signal from the selected channel is sampled, and the conversion process is initialed. While the conversion is in progress, the device outputs data at the same time. The 16-bit data word contains a 4-bit head data (which can be configured as channel address or GPIO status), followed by a 12-bit conversion resulting in MSB first format.

The device outputs DO15 (first bit of 4-bit head data) on the falling edge of CSN, and outputs DO14~DO0 on the subsequent falling edge of SCLK.

If the user configures the input channel to CHx in the [N-2]th frame. The device selects CHx on the 2nd SCLK falling edge in the [N-1]th frame. The device starts the acquisition phase of CHx on the 14th SCLK rising edge in the [N-1]th frame. The device ends the acquisition phase and samples the CHx signal on the CSN falling edge in the [N]th frame. And the device outputs the conversion result on the subsequent SCLK falling edge in the [N]th frame.

The device offers a 1X/2X input range feature. There are two ways to change the input range. The input range can be changed to 2X by writing DI06 = 1 in the mode control register; in this case, the register is written in on the 16th SCLK rising edge of this frame. Because the input range change is implemented by changing the sampling capacitor, the register takes effect in the acquisition phase in the next frame and affects the output conversion data in the third frame.

Another way to change the input range is through GPIO in the case of the TSSOP packaged devices. GPIO2 can act as the RangeSel input. The RangeSel signal takes effect in the next acquisition phase.

The TSSOP packaged devices have four General Purpose IO(GPIO) pins. These four pins can be individually programmed as GPO or GPI. It is also possible to use them for pre-assigned functions. GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the CSN falling edge as per the SDI data written in the previous frame.

Similarly, the device latches the GPI status on the CSN falling edge and outputs the GPI data on the SDO line in the same frame starting with the CSN falling edge.

The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits, the device flags out an alarm on GPIO0/GPIO1 depending on the GPIO program register setting. The alarm is asserted (under the alarm conditions) on the 12th SCLK falling edge in the same frame when data conversion is in progress. The alarm outputs are reset on the 10th falling edge of SCLK in the next frame.

The device offers a power-down feature to save power when not in use. There are two ways to power down the device. It can be powered down by writing DI05 = 1 in the mode control register; in this case the device powers down on the 16th falling edge of SCLK in the next frame. The device will power up again with DI05 = 0 in the mode control register.

E.g. if the user configures mode control register DI05 = 1 in the [N-2]th frame. The register writes in on the 16th SCLK rising edge in the [N-2]th frame. ADC works properly in the [N-1]th frame. The device powers down ADC on the 16th SCLK falling edge in the [N-1]th frame. The device goes into a power-down mode in the [N]th frame. And if the user configures mode control register DI05 = 0 in the [N+1]th frame. The register writes in on the 16th SCLK rising edge in the [N+1] th frame, and the device powers on in the [N+1]th frame. After 1 frame analog settling time, the ADC works properly in the [N+2]th frame.

Another way to power down the device is through GPIO in the case of the TSSOP packaged devices. GPIO3 can act as the PDN input. This is an asynchronous and active low input. The device powers down instantaneously after GPIO3(PDN) = 0.

Functional Block Diagram

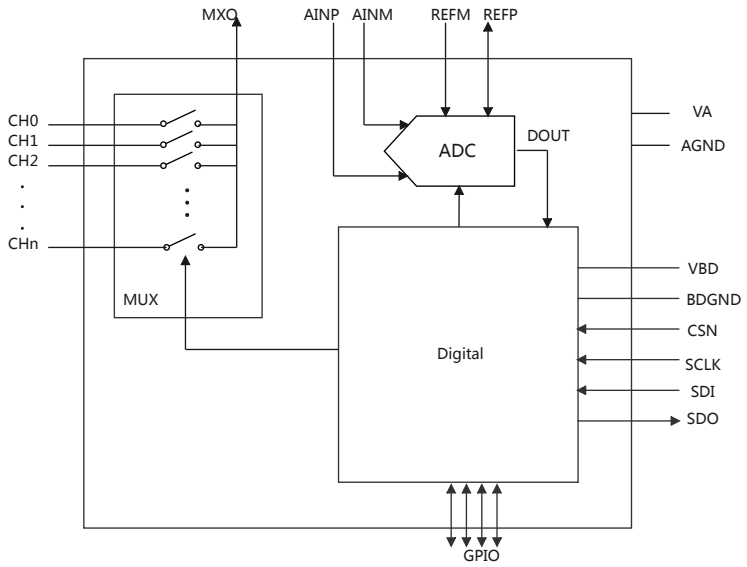


Figure 10. TPC5120Q Block Diagram

Feature Description

Device Functional Modes

Channel Sequencing Modes

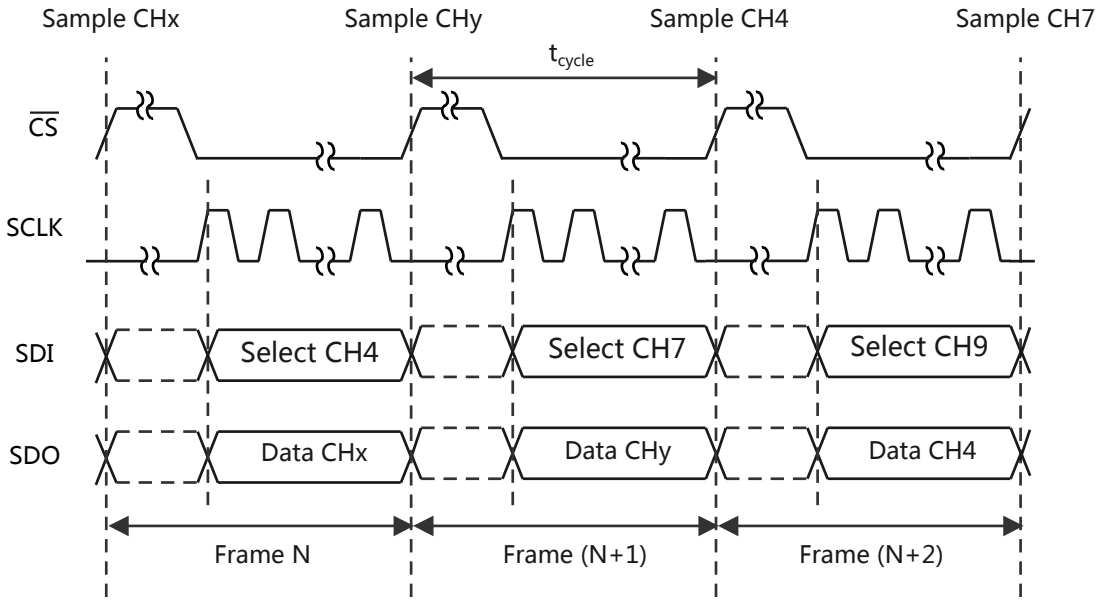


Figure 11. Example Manual Mode Timing Diagram

Table 2. Mode Control Register Settings for Manual Mode

Bits	Reset State	Logic State	Function
DI15-12	0001	0001	Select Manual Mode
DI11	0	1	Enable programming of bits DI06-00
		0	Device retains values of DI06-00 from the previous frame
DI10-07	0000		This four-bit data represents the address of the next channel to be selected in the next frame. DI10: MSB and DI07: LSB. For example, 0000 represents channel- 0, 0001 represents channel-1 and so forth.
DI06	0	0	Select 0 to V_{REF} input range (Range 1)
		1	Select 0 to 2 x V_{REF} input range (Range 2)
DI05	0	0	Device norma operation (no power-down)
		1	Device powers down on the 16th SCLK falling edge
DI04	0	0	SDO outputs the current channel address of the channel on DO15..12 followed by 12 bit conversion result on DO11..00
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.

Bits	Reset State	Logic State	Function			
			DOI5	DOI4	DOI3	DOI2
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000		GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below			
			DOI3	DOI2	DOI1	DOI0
			GPIO3	GPIO2	GPIO1	GPIO0

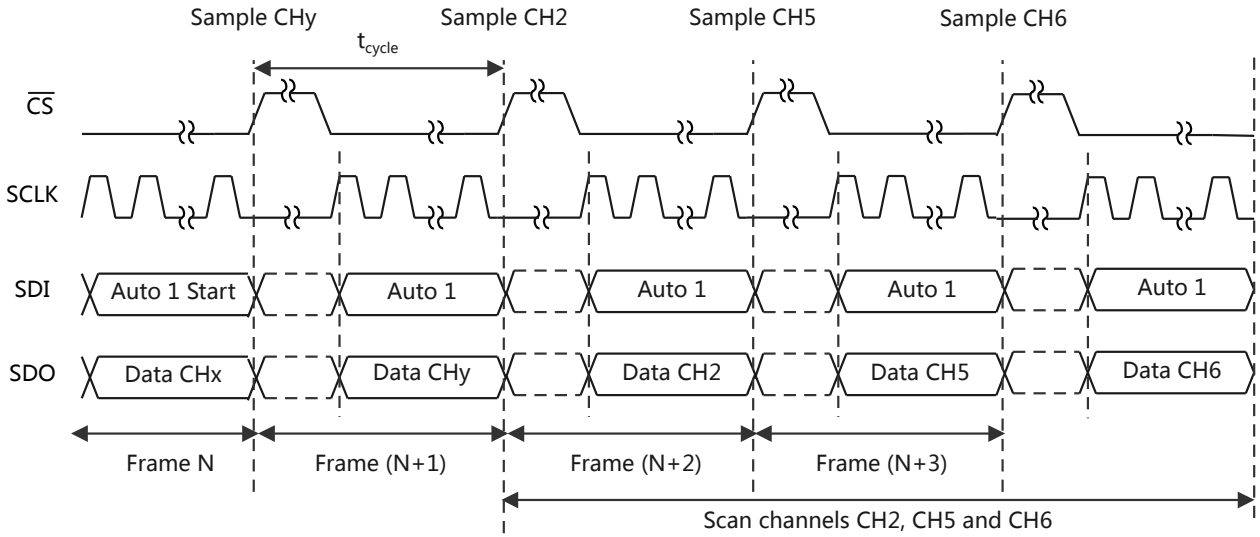


Figure 12. Example Auto-1 Mode Timing Diagram

Table 3. Mode Control Register Settings for Auto-1 Mode

Bits	Reset State	Logic State	Function
DI15-12	0001	0010	Select Auto-1 Mode
DI11	0	1	Enable programming of bits DI10-00.
		0	Device retains values of DI10-00 from the previous frame.
DI10	0	1	The channel counter is reset to the lowest programmed channel in the Auto-1 Program Register
		0	The channel counter increments every conversion (No reset)
DI09-07	000	xxx	Do not care
DI06	0	0	Select 0 to V_{REF} input range (Range 1)
		1	Select 0 to 2 x V_{REF} input range (Range 2)
DI05	0	0	Device normal operation (no power down)
		1	Device powers down on the 16th SCLK falling edge

Bits	Reset State	Logic State	Function			
DI04	0	0	SDO outputs the current channel address of the channel on DO15..12 followed by a 12-bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000		GPIO data for the channels configured as output. The device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information are given below			
			DI03	DI02	DI01	DI00
			GPIO3	GPIO2	GPIO1	GPIO0

Table 4. Program Register Settings for Auto-1 Mode

Bits	Reset State	Logic State	Function
FRAME 1			
DI15-12	NA	1000	The device enters the Auto-1 program sequence. Device programming is done in the next frame.
DI11-00	NA	Do not care	
FRAME 2			
DI15-00	All 1s	1 (individual bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example, DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00
		0 (individual bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00

Table 5. Mapping of Channels to SDI Bits for 16, 12, 8, 4 Channel Devices

Device (1)	SDI BITS															
	DI15	DI14	DI13	DI12	DI11	DI10	DI09	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DI00
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
12 Chan	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
8 Chan	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
4 Chan	X	X	X	X	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0

(1) When operating in Auto-1 mode, the device only scans the channels programmed to be selected.

Table 6. Mode Control Register Settings for Auto-2 Mode

Bits	Reset State	Logic State	Function			
DI15-12	0001	0011	Select Auto-2 Mode			
DI11	0	1	Enable programming of bits DI10-00.			
		0	Device retains values of DI10-00 from the previous frame.			
DI10	0	1	Channel number is reset to Ch-00.			
		0	Channel counter increments every conversion.(No reset).			
DI09-07	000	xxx	Do not care			
DI06	0	0	Select V_{REF} i/p range (Range 1)			
		1	Select 2 x V_{REF} i/p range (Range 2)			
DI05	0	0	Device normal operation (no power down)			
		1	Device powers down on the 16th SCLK falling edge			
DI04	0	0	SDO outputs the current channel address of the channel on DO15..12 followed by the 12-bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000		GPIO data for the channels configured as output. Device ignores data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below			
			DI03	DI02	DI01	DI00
			GPIO3	GPIO2	GPIO1	GPIO0

Table 7. Program Register Settings for Auto-2 Mode

Bits	Reset State	Logic State	Function
DI15-12	NA	1001	Auto-2 program register is selected for programming
DI11-10	NA	Do not care	
DI09-06	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in Auto-2 mode, the channel counter starts at CH-00 and increments every frame until it equals "aaaa". The channel counter rolls over to CH-00 in the next frame.
DI05-00	NA	Do not care	

Table 8. Continued Operation in a Selected Mode

Bits	Reset State	Logic State	Function
DI15-12	0001	0000	The device continues to operate in the selected mode. In Auto-1 and Auto-2 modes the channel counter increments normally, whereas in the Manual mode it continues with the last selected channel. The device ignores data on DI11-DI00 and continues operating as per the previous settings. This feature is provided so that SDI can be held low when no changes are required in the Mode Control Register settings.
DI11-00	All '0'	The device ignores these bits when DI15-12 is set to 0000 logic state	

Programming

Digital Output

As discussed previously in Overview, the digital output of the devices is SPI compatible. The following tables list the output codes corresponding to various analog input voltages.

Table 9. Ideal Input Voltages and Output Codes

Description		Analog Value	Digital Output	
Full-scale range	Range 1 → V_{REF}	Range 2 → 2×V_{REF}	STRAIGHT BINARY	
The least significant bit (LSB)	V_{REF} / 4096	2V_{REF} / 4096	BINARY CODE	HEX CODE
Full scale	V_{REF} – 1 LSB	2V_{REF} – 1 LSB	1111 1111 1111	FFF
Midscale	V_{REF} / 2	V_{REF}	1000 0000 0000	800
Midscale – 1 LSB	V_{REF} / 2 – 1 LSB	V_{REF} – 1 LSB	0111 1111 1111	7FF
Zero	0 V	0 V	0000 0000 0000	000

Table 10. GPIO Program Register Settings

Bits	Reset State	Logic State	Function
DI15-12	NA	0100	Device selects GPIO Program Registers for programming.
DI11-10	00	00	Do not program these bits to any logic state other than ‘00’
DI09	0	1	Device resets all registers in the next $\overline{CS}$ frame to the reset state shown in the corresponding tables (it also resets itself).
		0	Device normal operation
DI08	0	1	Device configures GPIO3 as the device power-down input.
		0	GPIO3 remains general purpose I or O. Program 0 for QFN packaged devices.
DI07	0	1	Device configures GPIO2 as device range input.
		0	GPIO2 remains general purpose I or O. Program 0 for QFN packaged devices.

Bits	Reset State	Logic State	Function
DI06-04	000	000	GPIO1 and GPIO0 remain general purpose I or O. Valid settings for QFN packaged devices.
		xx1	Device configures GPIO0 as 'high or low' alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		010	Device configures GPIO0 as high alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		100	Device configures GPIO1 as low alarm output. This is an active high output. GPIO0 remains general purpose I or O. Setting not allowed for QFN packaged devices.
		110	Device configures GPIO1 as low alarm output and GPIO0 as a high alarm output. These are active high outputs. Setting not allowed for QFN packaged devices.
Note: The following settings are valid for GPIO which are not assigned a specific function through bits DI08..04			
DI03	0	1	GPIO3 pin is configured as a general-purpose output. Program 1 for QFN packaged devices.
		0	GPIO3 pin is configured as a general-purpose input. Setting not allowed for QFN packaged devices.
DI02	0	1	GPIO2 pin is configured as a general-purpose output. Program 1 for QFN packaged devices.
		0	GPIO2 pin is configured as a general-purpose input. Setting not allowed for QFN packaged devices.
DI01	0	1	GPIO1 pin is configured as a general-purpose output. Program 1 for QFN packaged devices.
		0	GPIO1 pin is configured as a general-purpose input. Setting not allowed for QFN packaged devices.
DI00	0	1	GPIO0 pin is configured as a general-purpose output. Valid setting for QFN packaged devices.
		0	GPIO0 pin is configured as a general-purpose input. Valid setting for QFN packaged devices.

Table 11. Grouping of Alarm Program Registers

Group No.	Registers	Applicable for Device
0	High and low alarm for channels 0, 1, 2, and 3	TPC5120Q
1	High and low alarm for channels 4, 5, 6, and 7	TPC5120Q
2	High and low alarm for channels 8, 9, 10, and 11	TPC5120Q
3	High and low alarm for channels 12, 13, 14, and 15	TPC5120Q

Table 12. Alarm Program Register Settings

Bits	Reset State	Logic State	Function
FRAME 1			
DI15-12	NA	1100	Device enters ‘alarm programming sequence’ for group 0
		1101	Device enters ‘alarm programming sequence’ for group 1
		1110	Device enters ‘alarm programming sequence’ for group 2
		1111	Device enters ‘alarm programming sequence’ for group 3
Note: DI15-12 = 11bb is the alarm programming request for group bb. Here ‘bb’ represents the alarm programming group number in binary format.			
DI11-14	NA	Do not care	
FRAME 2 AND ONWARDS			
DI15-14	NA	cc	Where “cc” represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number “bbcc”. “bb” is programmed in the first frame.
DI13	NA	1	High alarm register selection
		0	Low alarm register selection
DI12	NA	0	Continue alarm programming sequence in next frame
		1	Exit Alarm Programming in the next frame. Note: If the alarm programming sequence is not terminated using this feature then the device will remain in the alarm programming sequence state and all SDI data will be treated as alarm thresholds.
DI11-10	NA	xx	Do not care
DI09-00	All 1s for high alarm register and all 0s for low alarm register	This 10-bit data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit word of the 12-bit conversion result. The device sets off an alarm when the conversion result is higher (High Alarm) or lower (Low Alarm) than this number. For 10-bit devices, all 10 bits of the conversion result are compared with the set threshold. For 8-bit devices, all 8 bits of the conversion result are compared with DI09 to DI02, and DI00, and 01 are 'do not care'.	

Register

Table 13. Register Map

Address	Type	Default	Register Name
4'b0000	W	12'h000	Continued Operation in a Selected Mode
4'b0001	R/W	12'h000	Manual Mode Control Register
4'b0010	R/W	12'h000	Auto-1 Mode Control Register
4'b0011	R/W	12'h000	Auto-2 Mode Control Register
4'b0100	R/W	12'h000	GPIO Program Register
4'b0101	/	12'h000	Reserved and forbidden to read/write.
4'b0110	/	12'h000	Reserved and forbidden to read/write.
4'b0111	R/W	12'h000	Reference enable. Not available for TPC5120Q
4'b1000	R/W	16'hffff	Auto-1 Mode Program Register
4'b1001	R/W	12'h3c0	Auto-2 Mode Program Register
4'b1100	W		Group0 Alarm Program Register
2'b00	R/W	10'h3ff	Channel0 High Alarm Register
	R/W	10'h000	Channel0 Low Alarm Register
2'b01	R/W	10'h3ff	Channel1 High Alarm Register
	R/W	10'h000	Channel1 Low Alarm Register
2'b10	R/W	10'h3ff	Channel2 High Alarm Register
	R/W	10'h000	Channel2 Low Alarm Register
2'b11	R/W	10'h3ff	Channel3 High Alarm Register
	R/W	10'h000	Channel3 Low Alarm Register
4'b1101	W		Group1 Alarm Program Register
2'b00	R/W	10'h3ff	Channel4 High Alarm Register
	R/W	10'h000	Channel4 Low Alarm Register
2'b01	R/W	10'h3ff	Channel5 High Alarm Register
	R/W	10'h000	Channel5 Low Alarm Register
2'b10	R/W	10'h3ff	Channel6 High Alarm Register
	R/W	10'h000	Channel6 Low Alarm Register
2'b11	R/W	10'h3ff	Channel7 High Alarm Register
	R/W	10'h000	Channel7 Low Alarm Register
4'b1110	W		Group2 Alarm Program Register
2'b00	R/W	10'h3ff	Channel8 High Alarm Register
	R/W	10'h000	Channel8 Low Alarm Register
2'b01	R/W	10'h3ff	Channel9 High Alarm Register
	R/W	10'h000	Channel9 Low Alarm Register

Address	Type	Default	Register Name
2'b10	R/W	10'h3ff	Channel10 High Alarm Register
	R/W	10'h000	Channel10 Low Alarm Register
2'b11	R/W	10'h3ff	Channel11 High Alarm Register
	R/W	10'h000	Channel11 Low Alarm Register
4'b1111	W		Group3 Alarm Program Register
2'b00	R/W	10'h3ff	Channel12 High Alarm Register
	R/W	10'h000	Channel12 Low Alarm Register
2'b01	R/W	10'h3ff	Channel13 High Alarm Register
	R/W	10'h000	Channel13 Low Alarm Register
2'b10	R/W	10'h3ff	Channel14 High Alarm Register
	R/W	10'h000	Channel14 Low Alarm Register
2'b11	R/W	10'h3ff	Channel15 High Alarm Register
	R/W	10'h000	Channel15 Low Alarm Register

RegisterI dentification

Table 14.

Manual Mode Control Register (4'b0001)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	ManuLSBEn	ManuChnl[3]	ManuChnl[2]	ManuChnl[1]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Manu Chnl[0]	Manu RangSel	Manu Pd	Manu GPIOEn	Manu GPIOData[3]	Manu GPIOData[2]	Manu GPIOData[1]	Manu GPIOData[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 15.

Auto-1 Mode Control Register (4'b0010)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	Auto1LSBEn	Auto1ChnlRst	NA	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NA	Auto1 RangSel	Auto1 Pd	Auto1 GPIOEn	Auto1 GPIOData[3]	Auto1 GPIOData[2]	Auto1 GPIOData[1]	Auto1 GPIOData[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 16.

Auto-2 Mode Control Register (4'b0011)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	Auto2LSBEn	Auto2ChnlRst	NA	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NA	Auto2 RangSel	Auto2 Pd	Auto2 GPIOEn	Auto2 GPIOData[3]	Auto2 GPIOData[2]	Auto2 GPIOData[1]	Auto2 GPIOData[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 17.

GPIO Program Register (4'b0100)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	1'b0	1'b0	GPIO RegRst	GPIO3 PdIn
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GPIO2 RangeIn	GPIO10 Cfg[2]	GPIO10 Cfg[1]	GPIO10 Cfg[0]	GPIO3 Cfg	GPIO2 Cfg	GPIO1 Cfg	GPIO0 Cfg
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 18.

Auto-1 Mode Program Register (4'b1000)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Auto1 Chnl[15]	Auto1 Chnl[14]	Auto1 Chnl[13]	Auto1 Chnl[12]	Auto1 Chnl[11]	Auto1 Chnl[10]	Auto1 Chnl[9]	Auto1 Chnl[8]
1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Auto1 Chnl[7]	Auto1 Chnl[6]	Auto1 Chnl[5]	Auto1 Chnl[4]	Auto1 Chnl[3]	Auto1 Chnl[2]	Auto1 Chnl[1]	Auto1 Chnl[0]
1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

Table 19.

Auto-2 Program Register (4'b1001)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	NA	NA	Auto2 Chnl[3]	Auto2 Chnl[2]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Auto2 Chnl[1]	Auto2 Chnl[0]	NA	NA	NA	NA	NA	NA
1'b1	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 20.

Group0 Alarm Program Register (4'b1100)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNum LSB[1]	ChnlNum LSB[0]	HiAlarm RegSel	Alarm PgCont	NA	NA	Alarm Th[9]	Alarm Th[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Alarm Th[7]	Alarm Th[6]	Alarm Th[5]	Alarm Th[4]	Alarm Th[3]	Alarm Th[2]	Alarm Th[1]	Alarm Th[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 21.

Group1 Alarm Program Register (4'b1101)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNum LSB[1]	ChnlNum LSB[0]	HiAlarm RegSel	Alarm PgCont	NA	NA	Alarm Th[9]	Alarm Th[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Alarm Th[7]	Alarm Th[6]	Alarm Th[5]	Alarm Th[4]	Alarm Th[3]	Alarm Th[2]	Alarm Th[1]	Alarm Th[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 22.

Group2 Alarm Program Register (4'b1110)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNumLSB[1]	ChnlNumLSB[0]	HiAlarmRegSel	AlarmPgCont	NA	NA	AlarmTh[9]	AlarmTh[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AlarmTh[7]	AlarmTh[6]	AlarmTh[5]	AlarmTh[4]	AlarmTh[3]	AlarmTh[2]	AlarmTh[1]	AlarmTh[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 23.

Group3 Alarm Program Register (4'b1111)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
ChnlNum LSB[1]	ChnlNum LSB[0]	HiAlarm RegSel	Alarm PgCont	NA	NA	Alarm Th[9]	Alarm Th[8]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Alarm Th[7]	Alarm Th[6]	Alarm Th[5]	Alarm Th[4]	Alarm Th[3]	Alarm Th[2]	Alarm Th[1]	Alarm Th[0]
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Table 24.

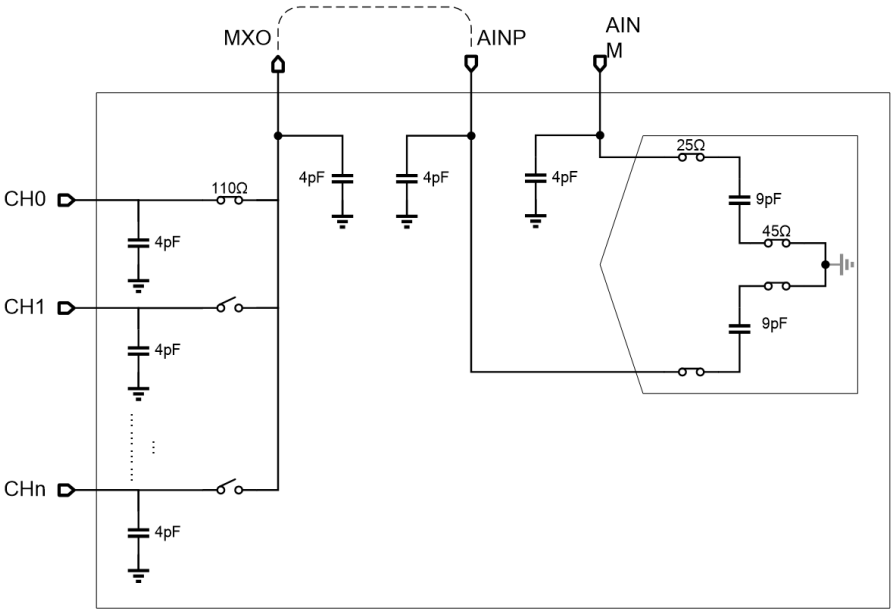
RefEn & FullDifEn Register (4'b0111)							
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
NA	NA	NA	NA	NA	NA	NA	NA
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NA	NA	NA	NA	NA	NA	RefEn	FullDifEn
1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information



In general application, the converting process is as below:

1. The multiplexer switch is on (meanwhile, the sampling switch is off, and ADC is in the conversion phase), and the channel input source charges the parasitic capacitor of MXO/AINP.
2. The sampling switch is on, and the 12-pF sampling capacitor (who is charged to the previously converted channel) is recharged to the current converting channel.
3. The sampling switch is off again. The sampling capacitor holds the signal, and the device goes into the conversion phase.
4. While the conversion is in progress, the device outputs data in the same time. Because the sampling switch is off, the multiplexer switch can switch to another channel freely on the 2nd SCLK rising edge in this phase.
5. Repeat 1~4.

Analog Input

There are about 22-pF internal capacitors in total. These capacitors consist of a pin parasitic capacitor and sampling capacitor. Before the multiplexer switch of the current converting channel closes, these capacitors are charged to the previous channel signal. These capacitors must settle to the current converting channel signal before the sampling switch opens. Several methods can be adopted to achieve enough performance.

1. Low impedance input source.
2. Large enough CHx decouple capacitor.

Users can tradeoff between source character, performance, and sampling rate, e.g. Assume that the source signal voltage is 2V, current saturation is less than 1.5V, source equivalent impedance is 1Kohms, and the resolution is 12bit. If the previous channel is 0V, and 22pF capacitor should be charged from 0V to 1.5V, and the step should be higher than 1 V. Then $C_{CHx} \times 2V + 22pF \times 0V > (C_{CHx} + 22pF) \times 1.5V$, $C_{CHx} > 66pF$, leave some guard band, 150pF decouple capacitor should be added to CHx. Be easy to calculate, all internal capacitor is charged in the Acquisition phase. At the beginning of Acquisition phase, charge balance between channel decouple capacitor and internal capacitor, the initial voltage is $(C_{CHx} \times 2V + C_{int} \times 2V) \div (C_{CHx} + C_{int}) = 1.7V$, and the final voltage is 2V, $\tau = 1k\Omega \times (150pF + 22pF) = 172ns$, and settling error less than 1LSB=610μV, Acquisition time should be longer than $\tau \times \ln((2V - 1.7V)/610\mu V) = 1.06\mu s$.

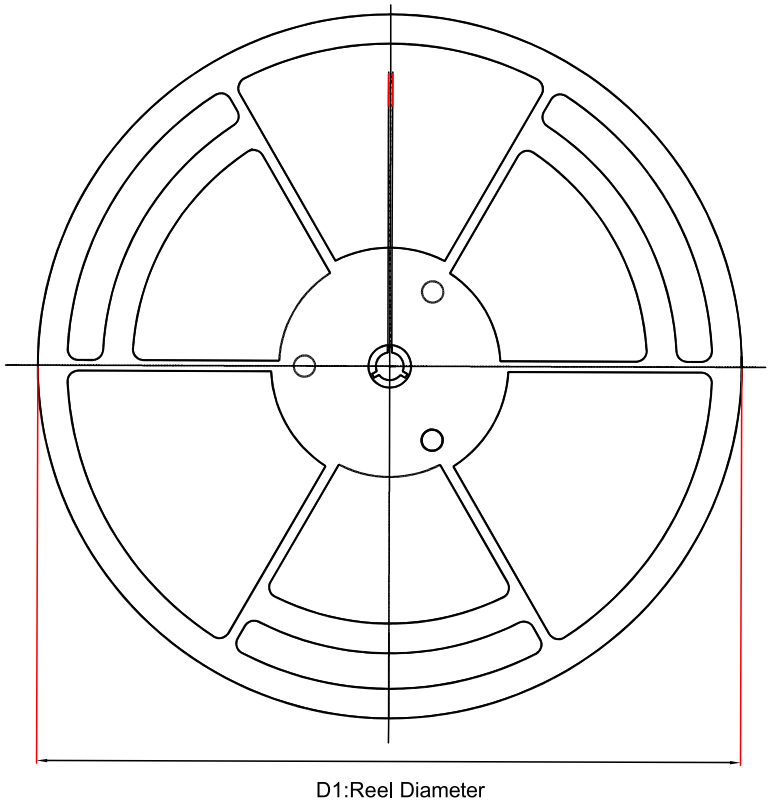
Reference

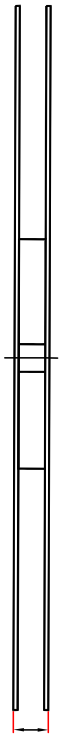
The TPC5120Q can operate with an external 2V ~ V_A reference. A clean, low-noise, low-output impedance, well-decoupled reference voltage on the REFP pin is required to ensure good performance. A 10μF ceramic decouple capacitor is required between the REFP and REFM pins of the converter. The capacitor should be placed as close as possible to the pins of the device. The connection between REFM and ground should be solid and should be avoided sharing any common path with another device. Because reference input resistance of this device is about 16 kohms, the sum of reference output resistance and total parasitic resistance of REFP and REFM should be less than 4ohms (which is easy to achieve with the careful layout).

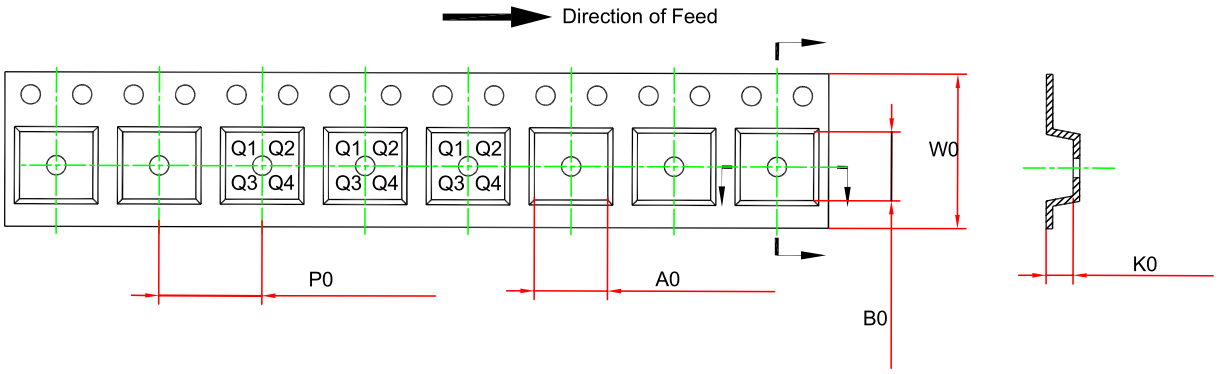
SPI Interface

The device converts input and output conversion results simultaneously. In order to reduce the effect of SPI output flipping, the drive capability of this device is weaker than other parts. So lighter SDO capacitive loading is required (less than 20pF) in high-speed application.

Tape and Reel Information





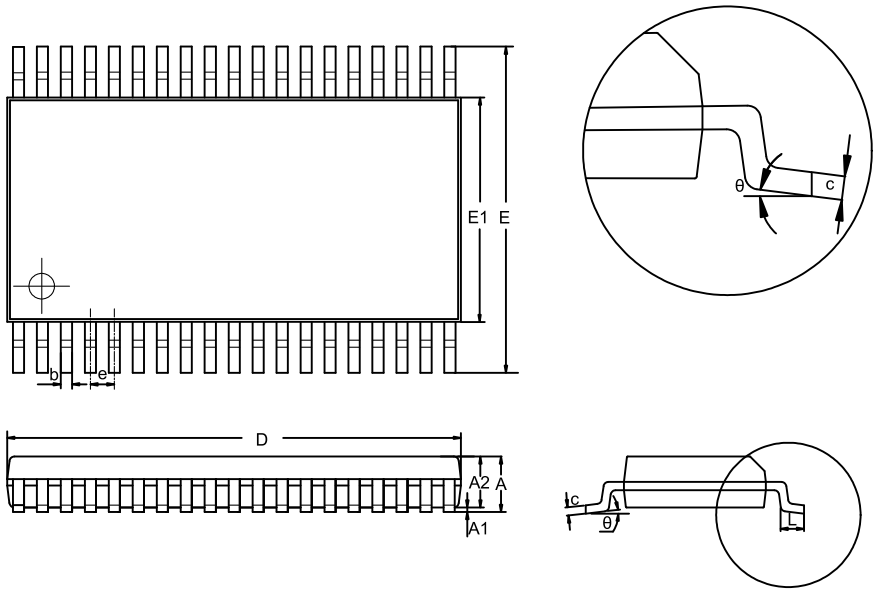


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC5120Q-TS7R-S	TSSOP-38	330	30.4	6.8	10.25	1.4	8	24	Q1

Package Outline Dimensions

TSSOP-38

Package Outline Dimensions TS7(TSSOP-38-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.200	---	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
e	0.500 BSC		0.020 BSC	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC5120Q-TS7R-S	−40 to 125°C	TSSOP-38	5120	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Copyright© 3PEAK 2012-2024. All rights reserved.

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.